ELEC4123

Electrical Design Proficiency

Term 1, 2023

Course Overview

Staff Contact Details

Convenors

Name	Email	Availability	Location	Phone
Arash Khatamianfar	a.khatamianfar@unsw.edu.au	By appointment	Room 313, EE&T Building (G17)	+61 2 9385 5231

School Contact Information

Consultations: Lecturer consultation times will be advised during the first lecture. You are welcome to email the tutor or laboratory demonstrator, who can answer your questions on this course and can also provide you with consultation times. ALL email enquiries should be made from your student email address with ELEC/TELExxxx in the subject line; otherwise they will not be answered.

Keeping Informed: Announcements may be made during classes, via email (to your student email address) and/or via online learning and teaching platforms – in this course, we will use Moodle https://moodle.telt.unsw.edu.au/login/index.php. Please note that you will be deemed to have received this information, so you should take careful note of all announcements.

Student Support Enquiries

For enrolment and progression enquiries please contact Student Services

Web

Electrical Engineering Homepage

Engineering Student Support Services

Engineering Industrial Training

UNSW Study Abroad and Exchange (for inbound students)

UNSW Future Students

Phone

(+61 2) 9385 8500 – Nucleus Student Hub

(+61 2) 9385 7661 – Engineering Industrial Training

(+61 2) 9385 3179 – UNSW Study Abroad and UNSW Exchange (for inbound students)

Email

Engineering Student Support Services – current student enquiries

- e.g. enrolment, progression, clash requests, course issues or program-related queries

Engineering Industrial Training – Industrial training questions

UNSW Study Abroad – study abroad student enquiries (for inbound students)

UNSW Exchange – student exchange enquiries (for inbound students)

UNSW Future Students – potential student enquiries

- e.g. admissions, fees, programs, credit transfer

Course Details

Units of Credit 6

Summary of the Course

The course involves three core design competency components, as follows:

- Electronic Circuit: Devices, amplifiers, tuned circuits, op-amp circuits, digital circuits, etc.
- Control System: Feedback and stability, linear control, data acquisition and sampling, etc.
- Signal Processing: Filter design, frequency response, spectrum analysis, BIBO analysis, etc.

The elective component of the course involves competency components in at least one of the following areas:

- Power System Design: Transformer, motor, power converter, power factor, harmonics, etc.
- Networked Communications: Computer programming, socket programming, network protocols, distributed asynchronous systems, estimation and exploitation of local and system-wide timing information, etc.
- Physical Communications: Modulation schemes, robust detection of signals in noise, multiplexing and interference suppression, efficient bandwidth utilization, error control, etc.
- Analog Design: Power amplifiers for audio systems, analog filters, linear system design, etc.

Laboratory assessment requires the design, construction and understanding of working solutions to specified problems.

Note: The components in core and elective topics may vary depending on the resources available in each term.

Course Aims

This is a rather unusual course, in that there is no final or mid-term examination and most of your contact hours are spent in the laboratory. The course is organized around **4 proficiency topics**, each of which has **four/4 formal lab sessions** lasting **3 or 4 hours** (depending on the logistics of the term offering). The **first three topics** cover the **core disciplines** of **Electronics**, **Signal Processing** and **Control Systems** (the order might change), while the **fourth topic** involves an **elective** choice of two or three different projects. With some exceptions for the elective topic, all formal lab sessions are assessment opportunities.

The **principle purpose** of this course is to test your **design proficiency**, through a sequence of design challenges. Some of the challenges are very basic, but there is also plenty of scope for you to demonstrate superior skills. The design challenges within each of the **core (non-elective) topics** are organized into **4 or 5 tasks** that can be undertaken and **assessed progressively**. In a normal setting (face-to-face delivery mode) your designs, implementation and assessment for the **core topics** are to be undertaken on an **individual basis**. But in some **unforeseen circumstances** you may be allowed to be **working in pairs**. However, you will still be **assessed individually** on your **understating** and **design decisions**. Moreover, you are expected to regard the laboratory sessions as **miniature examinations**.

A **secondary aim** of the course is to **fill in any major holes** in your **fundamental design knowledge**,

to ensure that all graduating students have at least a **minimum level of proficiency**. Although some of you might initially feel uncomfortable about this, it is important to realise that prospective employers will be very pleased indeed to know that you are able to demonstrate your proficiency. You should expect that this course will **reinforce** your **existing knowledge** and **increase** your **confidence in design** and some of the fundamental disciplines you have been studying. Opportunities to correct misunderstandings mostly occur between laboratory sessions and/or tutorial/consultation sessions.

A **third and final objective** of the course is to expose you to a healthy balance between **teamwork** and **individual responsibility**. Team-based design work is primarily reserved for the elective topic. However, for practical reasons and situational factors (as mentioned above) this could be extended to core topics as well while the individual aspect of design work will still be assessed. The elective topic will involve both individual and group assessment components. You will be assigned a tutor who can both help to keep you on track and also keep an eye on the functioning of your team and the level of contribution that each team member appears to be making to the design.

In summary, the aims of the course are:

1. Provide the student with a realistic design experience.
2. Ensure the students design skills are adequate and to the level desirable for a graduate engineer.
3. Give the student the opportunity to address weaknesses in their design skill base and to advance this skill base.
4. Prepare the students for the transition from the learning environment to the professional setting where these design skills are essential.

Course Learning Outcomes

After successfully completing this course, you should be able to:

Learning Outcome	**EA Stage 1 Competencies**
1. Demonstrate an ability to work both individually and within a group.	PE3.1, PE3.2, PE3.3, PE3.4, PE3.5, PE3.6
2. Produce designs which draw upon a number of disciplines previously studied in other courses.	PE1.3, PE1.5, PE2.1, PE2.2, PE2.3, PE2.4, PE3.1, PE3.2, PE3.3, PE3.4, PE3.5, PE3.6
3. Demonstrate the ability to contribute to and learn from peers.	PE1.3, PE1.5, PE2.1, PE2.2, PE2.3, PE2.4, PE3.1, PE3.2, PE3.3, PE3.4, PE3.5, PE3.6
4. Develop a sufficient level of understanding and engineering design skills within a range of disciplines.	PE1.3, PE1.5, PE2.1, PE2.2, PE2.3, PE2.4, PE3.1, PE3.2, PE3.3, PE3.4, PE3.5, PE3.6
5. Explain, evaluate, and reflect on design decisions and well as implementing them to achieve the design requirements.	PE1.3, PE1.5, PE2.1, PE2.2, PE2.3, PE2.4, PE3.1, PE3.2, PE3.3, PE3.4, PE3.5, PE3.6

Teaching Strategies

Delivery Mode

The teaching in this subject is heavily focused on laboratories. Each of **4 design topics** has **4 assigned laboratories**, (there could be optional open labs in face-to-face mode). The laboratories are designed to develop and assess proficiency in each discipline of electrical engineering.

Note: In this term, **you will be doing core topics individually.**

Consultation times are scheduled for **1 hour** each week with a **dedicated tutor/mentor**. They are intended to provide an opportunity to both address knowledge gaps and also to reinforce an approach to design which focuses on **the need to identify early what is most problematic about a design problem**. Through this process, students are expected to be better prepared to approach the larger design problem that they will face as a team during the elective design topic.

Please note that **MS Teams** will be used as the main platform for the course (the first page of this document is auto-generated and may not reflect the new changes). Through these mechanisms, the course aims to build and ensure proficiency in the core areas of your program of study.

Design Topics

The course is divided into **three core design topics** and **one elective design topic**, each of which is assigned **four/4** formal laboratory sessions. The **core design topics** are Signal Processing, Electronic Circuits and Control System (order may be subjected to change). For the Electronics topic, there will be a extra week dedicated to **PCB design tasks**. The **elective topics** are: Topic 4a: Energy Systems; Topic 4b: Data Networks; and Topic 4c: Telecommunications. Topic 4d: Analog Design.

Disclaimer: Due to situational factors, not all the elective topics may be offered this course.

Each of the core topics consists of a sequence of design tasks, with progressively higher complexity. Regardless of the core topics being allowed to be completed in pairs or individually, the major portion of the assessment is based on your **individual contribution** to the design, implementation and understanding regardless of working in pairs.

The elective design is performed in **groups** of **4 students**. You must **nominate** which of the **elective topics** you intend to pursue **before the end of Week 7** when the final available elective topics are released earlier in that week, at which point you will also have an opportunity to propose a design team. If you are not part of a proposed team, or if unavoidable circumstances require it, you will be assigned to a team at the course convener's discretion. You will be provided with further instructions on how to submit elective topic and team nominations. Unlike the first three design topics, the **elective design is assessed only in the final week**, however, the **progressive observation** of the **team performance** and **individual contribution** to the project is carried out by the lab demonstrators acting as mentors to help better assess the teams in the final week.

Individual Learning

Preparation for labs is essential to success in this course. You should find yourself revising material from previous courses, discussing problems with your peers and lab partner, raising questions in consultation times, and perhaps struggling to find and solve problems you encounter with your design.

Group Learning

You are encouraged to discuss the design tasks with your classmates outside the laboratory sessions. But you **MUST NOT** under any circumstances **collude with other groups** and **use identical design**, **pay someone to do the work for you**, and **ask a friend who have done this course to do your work for you**. If we catch you cheating, you will be **punished** heavily according to UNSW Plagiarism Policies, something that is not worth going through knowing the **pain and the trauma** that it would cause you and the permanent black mark next to your name in your official record.

The elective topic is a team effort, having larger scope and less incremental objectives than the first three design topics. To succeed in this topic, you will need to work effectively as a team member or leader. Moreover, each team is required to submit a report describing the design principles, implementation, outcomes and final reflections. The report will also need to be a team effort.

Laboratory Exemption

There is **no laboratory exemption** for this course. Regardless of whether equivalent labs have been completed in previous courses, all students enrolled in this course must take the labs. If, for medical reasons, (note that a valid medical certificate must be provided) you are unable to attend a lab, you will need to **seek permission from the Course Convener** to be assessed in a subsequent week upon providing legitimate documents.

Additional Course Information

Credits

This is a 6 UoC course. Since this course has **no final examination**, the workload of the course is compacted into just 10 weeks, so your effort must be adjusted accordingly. In addition to the official allocated formal lab hours in this course (8hrs/w or 6hrs/w), you must be aware of the fact that the nature of this course requires **much higher workload** than any normal courses you have had in your degree. Therefore, you must be prepared to manage your study load accordingly for independent study, design and preparation. This is not only an expectation, it is a reality that most students undertaking this course do put in a large amount of time, so you should expect even more workload for this course!! If you have any concern or complaint about the workload for this course, please raise them directly with the Head of School, because as the coordinator of this course my hands are tight.

Relationship to Other Courses

This is a 4th-year design course in the School of Electrical Engineering and Telecommunications, which is a core component of the BE and BE-ME programs (Electrical and Telecommunications) offered by the School. This course directly ties into core courses in Electronics, Signal Processing, Control, Telecommunications, Data Networks and Energy and Power Systems which you should have already taken (typically in the third year of your program). See below for more on what is expected.

Pre-requisites and Assumed Knowledge

In addition to **DESN1000** and **ELEC3117**, the knowledge from the courses below is **essential**:

- Electronics (to the level of **ELEC3106**, **ELEC2141** and **ELEC2133**).
- Signal Processing (to the level of **ELEC3104**)
- Control Systems (to the level of **ELEC3114**).

Through these and other courses, it is assumed that students have also developed good **programming/coding literacy** and familiarity with LTspice, MATLAB/Simulink as well as microcontroller which might be used in some topics.

Important note: If you **have NOT taken either of these courses**, you should reconsider your options as it is **NOT recommended** in any way or any form to take this course without having passed these courses. Even though there is no official pre-requisite for this, that does not mean you can take it before finishing all your 3rd-year core courses plus some 4th-year elective. It is your responsibility to make sure you have proper assume knowledge and pre-requisites for this course as there is no official design teaching or revision of pre-requisites in this course. It is also assumed that you have completed at least the **same UoCs** or even more as are required for **Thesis A** so that you are able to choose the right elective topic. They are heavily based on **4th-year elective courses** in your program.

Again, if you have any concern or complaint about the pre-requisites and assumed knowledge, please raise them directly with the Head of School, because as the coordinator of this course my hands are tight.

This is the course that is supposed to be taken at the end of your degree (with Thesis A , B or C after completing all your 3rd-year core courses plus some 4th-year electives). So you can demonstrate how much you have learned throughout your degree and prove to yourself how qualified you have become to be ready for the workforce after your graduation.

Assessment

Assessment of core design tasks

All completed tasks for the three core design topics are to be **assessed during the scheduled laboratory sessions** by one of the laboratory demonstrators. Once you have completed a task, you should add your name to a **marking form** so that you can be assessed as quickly as possible.
NOTE: You cannot expect to be assessed for all of the tasks you have completed during the final laboratory session of the topic, since this can place an unacceptable burden on the demonstrators time. As a result, we devised a plan for task assessment as follows:

- For each lab session, it is recommended that you complete **at least one task** and get it assessed, but **no more than two tasks will be marked**.
    - You are NOT allowed to put down your name for two tasks back-to-back. You have to first get assessed for the first task you complete, then you can put down your name again for the second task.
- Final assessment lab session: **No more than two tasks will be assessed**.
    - So please make sure to ***not leave your tasks pile up for the final lab session***.
- You will have **maximum 2 attempts** to get assessed for each task (there is no penalty attached to the second attempt).

Commonly Asked Questions: WHAT MARK DO I NEED TO GET FROM EACH TOPIC TO PASS THE COURSE? WHAT DO I HAVE TO DO TO GET HD FROM THIS COURSE? DO I HAVE TO CONTINUE WITH OTHER TASKS IF I KNOW I HAVE ALREADY ACHIEVED A PASSING MARK FROM THAT TOPIC? And more of these questions ....

Come to the first lecture to find out!!!!

Below is the breakdown of the marking strategy for **core topics** which covers **66%** of your total course mark (**22%** for each topic):

- **8%** of the topic mark is awarded based on **actual outcomes** and **satisfying the design requirements**. This will be known as ***Requirement and Soft Objectives mark*** (***Req+Soft***). You cannot expect to obtain any of these marks for a solution which does not actually work or achieve the task objectives to some extent. This item is a **group mark,** but it could be overridden (please read below).
- **12%** of the topic mark is awarded for your **understanding** of the **design problem** and your design approach. This is known as ***Understanding mark*** (***Und***). To obtain these marks, you will need to convince the assessor that you thoroughly understand your design and be able to justify your design decisions. This item is an **individual mark**.
- Please note that your Req+Soft mark will be usually **capped** by the Und mark and vice versa. But there are exceptions as explained below.
    - For example, you might have a fully functioning design that satisfies all the given requirements in a task, but you may not be able to explain the main reasons behind your design decisions, or demonstrate your understanding of the background knowledge required to come up with selected design, or not being able to answer to some specialized understanding questions around the relevant topic to the task. Under these circumstances, you Req mark is either capped by your Und mark (equal mark for both Req and Und) or Req could be only one mark higher than Und (this situation would mainly raise the suspicion of plagiarism and collusion, so be careful!!!)
    - In an opposite case where you do not have a functioning design, you should not expect to

receive a mark for Und higher than your Req mark. That mean you will receive equal mark for req and Und, unless you can explain why your design is not working as it should be and demonstrate a good deal of understating. Then your Und mark can be higher by one mark.

- At the end of each topic, you must submit a short **reflective task** worth **2%** by answering some questions to reflect on your work and learning gained from that topic.
    - The submission of this task is through Assignment section MS Teams (the deadline is mostly **last Sun before the next topic** begins at **11pm**).
    - The mark is awarded for your **genuine effort** in providing your **reflections** on your work on each topic (there is no right or wrong answer, but there is a **word limit**).

You **MUST maintain a lab book** (electronic or paper-based) to show all your design workings and observations during the assessment. At the end of each topic, you will receive your marks through Power Automate Chat-bot, in addition to on-the-spot marks written on your lab book.

Assessment of the elective design tasks

The elective design topic is a **group activity**, for which the **final assessment** will take place on **Fri of Week 10 or Mon of Week 11 (depending on situational factors and circumstances)**, but your **team performance** and **individual contribution** will be observed and assessed continuously by an **allocated lab demonstrator** to your group during lab sessions. Below is the breakdown of the marking strategy for the elective topic which covers **34%** of your total course mark:

- **22%** of the topic mark is awarded by the lab demonstrators in the final assessment day (and during **progress review** sessions).
    - **12%** is awarded based on an **individual interview** of **each team member**, to determine their level of **understanding** (Und) of both the overall design and their **individual contribution** to it.
    - **10%** is awarded based on the **achievement of the requirements** in the **final design** (Req), a component of which will be competitive, meaning that teams will be ranked within each topic, based on the objective performance of their designs.
- **7%** of the topic mark is awarded to your team's **final report.** This is an essential part of the reflective process.
    - You will be expected to have a **draft** version of the **report** available during the final assessment of the elective topic (this could include your workings, design strategies, figures, equations, anything that shows your effort in completing the analytical and practical part of the design task). However, the final version of the report should be finalized afterwards, including a reflection on the design process that you followed considering your final design performance. The report submission is **due on Sun of Week 11 at 11pm** (with a possibility of extension due to situational factors).
- **5%** of the topic mark is awarded to your **team performance**.

Each team will have a dedicated tutor/mentor. Regardless of in-person of online labs, you must provide a briefing on your progress to your mentor during the lab times. This is called **progress review**. Your mentor will schedule progress review times with their teams. Mentors will observe your team's interaction and thought processes, asking some questions, and offer suggestions where appropriate after you presented your progress. Your mentor will especially be interested in the way in which you approach the design problem, how you ensure that you **focus on the most challenging parts of the problem first**, how you reach an overall design that is likely to work, and how your team manages the resources at its disposal. Your mentor will also observe how individual members contribute to the team's deliberations, design, and interaction during elective topic scheduled lab sessions. Based on these observations, the

mentor will award **team performance** mark as well as your **individual contribution** which is part of your overall **understanding mark**.

Please **note** that **attending** these progress review sessions is **compulsory**.

Assessment task	Weight	Due Date	Course Learning Outcomes Assessed
1. Core Design Tasks and Individual Reflection	66%	See the Course Schedule	1, 2, 3, 4, 5
2. Elective Design Task	22%	See the Course Schedule	1, 2, 3, 4, 5
3. Elective Design Team Performance and Report	12%	Week 10-11 (See the Course Schedule)	1, 2, 3

Assessment 1: Core Design Tasks and Individual Reflection (Group)

Due date: See the Course Schedule

Assessment 1 Concept: Core Topics	Basis	Marks
Achievement of design requirements, as demonstrated in labs	Group or Individual	3x8% (24%)
Understanding of relevant subject material, as demonstrated in labs	Individual	3x12% (36%)
Reflective task, submitted online, core topics T1-T3	Individual	3x2% (6%)

Assessment 2: Elective Design Task (Group)

Due date: See the Course Schedule

Assessment 2 Concept: Elective Topic	Basis	Marks
Achievement of design requirements, as demonstrated in labs	Group	10%
Understanding of relevant subject material and individual contribution	Individual	12%

Assessment 3: Elective Design Team Performance and Report (Group)

Due date: Week 10-11 (See the Course Schedule)

Assessment 3 Concept: Elective Topic	Basis	Marks
Team performance	Group and Individual	5%
Team report	Group	7%

This assignment is submitted through Turnitin and students can see Turnitin similarity reports.

Attendance Requirements

Students are strongly encouraged to attend all classes and review lecture recordings.

Course Schedule

Indicative Laboratory Schedule (Tue and Fri are assessment labs)

Place: Lab rooms 201,224,225,119, G14. You will receive your allocated bench number and lab room before your first lab.

Consultations: Mon and Thu consultations for each topic will be recorded, including the introductory lecture. They might be run in person, which then the classroom will be announced in advance.

Open-labs: To accommodate more lab access time for students to work on their tasks, there will be open-lab times available throughout the week. The **tentative** schedule will be announced during the class in Week 1.

Elective Topic Progress Review: The progress review sessions will be during normal lab times.

View class timetable

Timetable

Date	Type	Content
Week 1: 13 February - 17 February	Lecture	• Mon 1pm-2pm: Introductory Lecture
	Laboratory	• Tue 3pm-7pm: Topic 1 - Signal Processing • Fri 3pm-7pm: Topic 1 - Signal Processing
Week 2: 20 February - 24 February	Laboratory	• Tue 3pm-7pm: Topic 1 - Signal Processing • Fri 3pm-7pm: Topic 1 - Signal Processing
Week 3: 27 February - 3 March	Laboratory	• Tue 3pm-7pm: Topic 2 - Electronics • Fri 3pm-7pm: Topic 2 - Electronics
Week 4: 6 March - 10 March	Laboratory	• Tue 3pm-7pm: Topic 2 - Electronics • Fri 3pm-7pm: Topic 2 - Electronics
Week 5: 13 March - 17 March	Laboratory	• Tue 3pm-7pm: Topic 2 - Electronics (PCB) • Fri 3pm-7pm: Topic 2 - Electronics (PCB)
Week 6: 20 March - 24 March	Laboratory	• Tue 3pm-7pm: Topic 3 - Control Systems • Fri 3pm-7pm: Topic 3 - Control Systems
Week 7: 27 March - 31 March	Laboratory	• Tue 3pm-7pm: Topic 3 - Control Systems • Fri 3pm-7pm: Topic 3 - Control Systems

Week 8: 3 April - 7 April	Laboratory	• Tue 3pm-7pm: Topic 4 - Electives • Fri 3pm-7pm: Topic 4 - Electives
Week 9: 10 April - 14 April	Laboratory	• Tue 3pm-7pm: Topic 4 - Electives • Fri 3pm-7pm: Topic 4 - Electives
Week 10: 17 April - 21 April	Laboratory	• Tue 3pm-7pm: Topic 4 - Electives • Fri 3pm-7pm: Topic 4 - Electives (Final Assessmnet, but it might be moved to Mon fo Week 11)

Resources

Prescribed Resources

There are no specific texts for this course, but you should consider your lecture notes and text books from earlier classes in Electronics, Signal Processing, Control, Telecommunications, Data Networks and/or Energy Systems to be useful resources.

Course Evaluation and Development

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the online student survey myExperience. You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings. As a result of previous feedback obtained for this course and in our efforts to provide a rich and meaningful learning experience, we have continued to evaluate and modify our delivery and assessment methods.

Academic Honesty and Plagiarism

Academic Honesty and Plagiarism

Plagiarism is the unacknowledged use of other people's work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a form of academic misconduct, and the University has very strict rules that include some severe penalties. For UNSW policies, penalties and information to help you avoid plagiarism, see https://student.unsw.edu.au/plagiarism. To find out if you understand plagiarism correctly, try this short quiz: https://student.unsw.edu.au/plagiarism-quiz.

General Conduct and Behaviour

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and students may be asked to leave the class.

Academic Information

COVID19 - Important Health Related Notice

Your health and the health of those in your class is critically important. You must stay at home if you are sick or have been advised to self-isolate by NSW health or government authorities. **You will not be penalised for missing a face-to-face activity due to illness or a requirement to self-isolate**. We will work with you to ensure continuity of learning during your isolation and have plans in place for you to catch up on any content or learning activities you may miss. Where this might not be possible, an application for fee remission may be discussed.

If you are required to self-isolate and/or need emotional or financial support, please contact the Nucleus: Student Hub. If you are unable to complete an assessment, or attend a class with an attendance or participation requirement, please let your teacher know and apply for special consideration through the Special Consideration portal. To advise the University of a positive COVID-19 test result or if you suspect you have COVID-19 and are being tested, please fill in this form.

UNSW requires all staff and students to follow NSW Health advice. Any failure to act in accordance with that advice may amount to a breach of the Student Code of Conduct. Please refer to the Safe Return to Campus guide for students for more information on safe practices.

Dates to note

Important Dates available at: https://student.unsw.edu.au/dates

Student Responsibilities and Conduct

Students are expected to be familiar with and adhere to all UNSW policies (see https://student.unsw.edu.au/policy), and particular attention is drawn to the following:

Workload

It is expected that you will spend at least **15 hours per week** studying a 6 UoC course, from Week 1 until the final assessment, including both formal classes and *independent, self-directed study*. In periods where you need to complete assignments or prepare for examinations, the workload may be greater. Over-commitment has been a common source of failure for many students. You should take the required workload into account when planning how to balance study with employment and other activities.

Attendance

Regular and punctual attendance at all classes is expected. UNSW regulations state that if students attend less than 80% of scheduled classes they may be refused final assessment.

Work Health and Safety

UNSW policy requires each person to work safely and responsibly, in order to avoid personal injury and to protect the safety of others.

Special Consideration and Supplementary Examinations

You must submit all assignments and attend all examinations scheduled for your course. You can apply for special consideration when illness or other circumstances beyond your control interfere with an assessment performance. If you need to submit an application for special consideration for an exam or assessment, you must submit the application **prior to the start** of the exam or before the assessment is submitted, except where illness or misadventure prevent you from doing so. Be aware of the "fit to sit/submit" rule which means that if you sit an exam or submit an assignment, you are declaring yourself well enough to do so and cannot later apply for Special Consideration. For more information and how to apply, see https://student.unsw.edu.au/special-consideration.

Administrative Matters

On issues and procedures regarding such matters as special needs, equity and diversity, occupational health and safety, enrolment, rights, and general expectations of students, please refer to the School and UNSW policies:

https://student.unsw.edu.au/guide

https://www.unsw.edu.au/engineering/our-schools/electrical-engineering-telecommunications/student-life/resources

Disclaimer

This Course Outline sets out description of classes at the date the Course Outline is published. The nature of classes may change during the Term after the Course Outline is published. Moodle should be consulted for the up-to-date class descriptions. If there is any inconsistency in the description of activities between the University timetable and the Course Outline (as updated in Moodle), the description in the Course Outline/Moodle applies.

Image Credit

The cover picture was taken by permission of concent of the School of EET and the student in the Lab EE201 while ELEC4123 was running.

CRICOS

CRICOS Provider Code: 00098G

Acknowledgement of Country

We acknowledge the Bedegal people who are the traditional custodians of the lands on which UNSW Kensington campus is located.

Appendix: Engineers Australia (EA) Professional Engineer Competency Standard

Program Intended Learning Outcomes	
Knowledge and skill base	
PE1.1 Comprehensive, theory based understanding of the underpinning natural and physical sciences and the engineering fundamentals applicable to the engineering discipline	
PE1.2 Conceptual understanding of the mathematics, numerical analysis, statistics, and computer and information sciences which underpin the engineering discipline	
PE1.3 In-depth understanding of specialist bodies of knowledge within the engineering discipline	✓
PE1.4 Discernment of knowledge development and research directions within the engineering discipline	
PE1.5 Knowledge of engineering design practice and contextual factors impacting the engineering discipline	✓
PE1.6 Understanding of the scope, principles, norms, accountabilities and bounds of sustainable engineering practice in the specific discipline	
Engineering application ability	
PE2.1 Application of established engineering methods to complex engineering problem solving	✓
PE2.2 Fluent application of engineering techniques, tools and resources	✓
PE2.3 Application of systematic engineering synthesis and design processes	✓
PE2.4 Application of systematic approaches to the conduct and management of engineering projects	✓
Professional and personal attributes	
PE3.1 Ethical conduct and professional accountability	✓
PE3.2 Effective oral and written communication in professional and lay domains	✓
PE3.3 Creative, innovative and pro-active demeanour	✓
PE3.4 Professional use and management of information	✓
PE3.5 Orderly management of self, and professional conduct	✓
PE3.6 Effective team membership and team leadership	✓