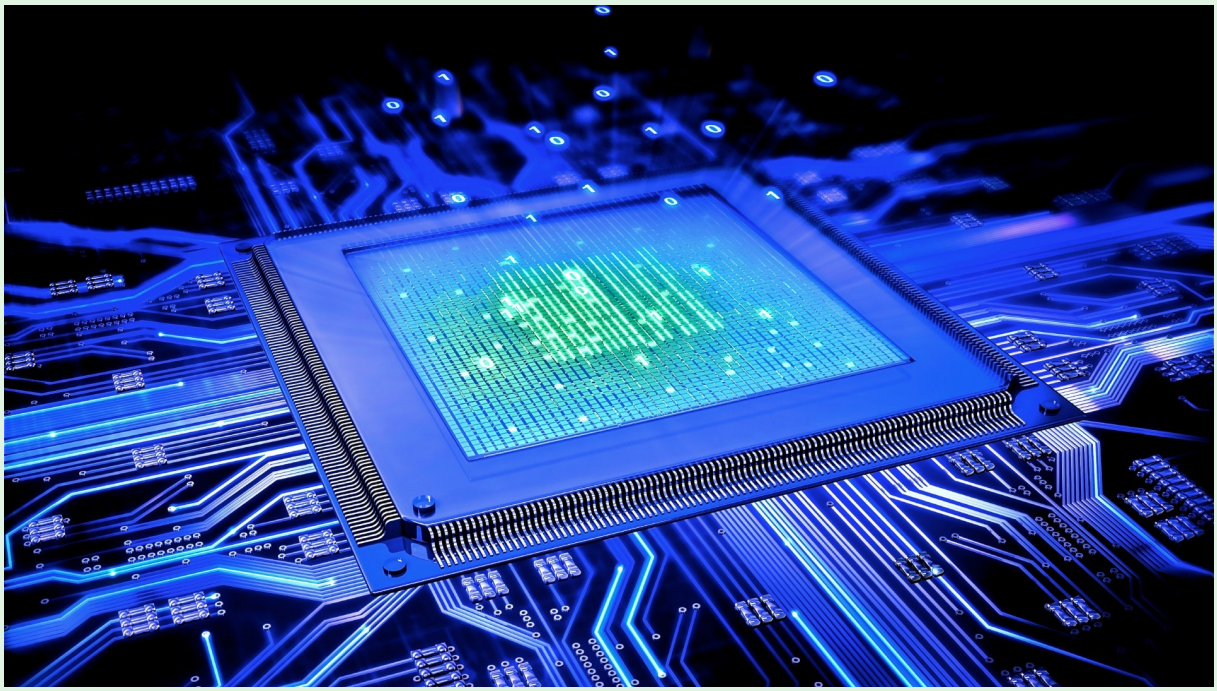
ELEC2141

Digital Circuit Design

Term 1, 2023



Course Overview

Staff Contact Details

Convenors

Name	Email	Availability	Location	Phone
Beena Ahmed	beena.ahmed@unsw.edu.au	Wed 12-2 pm	EE&T 444	

Tutors

Name	Email	Availability	Location	Phone
Waheeda Jabbar	w.jabbar@unsw.edu.au			

Lab Staff

Name	Email	Availability	Location	Phone
Jonah Meggs	j.meggs@unsw.edu.au			

School Contact Information

Consultations: Lecturer consultation times will be advised during the first lecture. You are welcome to email the tutor or laboratory demonstrator, who can answer your questions on this course and can also provide you with consultation times. ALL email enquiries should be made from your student email address with ELEC/TELExxxx in the subject line; otherwise they will not be answered.

Keeping Informed: Announcements may be made during classes, via email (to your student email address) and/or via online learning and teaching platforms – in this course, we will use Moodle https://moodle.telt.unsw.edu.au/login/index.php. Please note that you will be deemed to have received this information, so you should take careful note of all announcements.

Student Support Enquiries

For enrolment and progression enquiries please contact Student Services

Web

Electrical Engineering Homepage

Engineering Student Support Services

Engineering Industrial Training

UNSW Study Abroad and Exchange (for inbound students)

UNSW Future Students

Phone

(+61 2) 9385 8500 – Nucleus Student Hub

(+61 2) 9385 7661 – Engineering Industrial Training

(+61 2) 9385 3179 – UNSW Study Abroad and UNSW Exchange (for inbound students)

Email

Engineering Student Support Services – current student enquiries

- e.g. enrolment, progression, clash requests, course issues or program-related queries

Engineering Industrial Training – Industrial training questions

UNSW Study Abroad – study abroad student enquiries (for inbound students)

UNSW Exchange – student exchange enquiries (for inbound students)

UNSW Future Students – potential student enquiries

- e.g. admissions, fees, programs, credit transfer

Course Details

Units of Credit 6

Summary of the Course

Introduction to modern digital logic design, combinational logic, switch logic and basic gates, Boolean algebra, two-level logic, regular logic structures, multi-level networks and transformations, programmable logic devices, time response. Sequential logic, networks with feedback, basic latches and flip-flops, timing methodologies, registers and counters, programmable logic devices. Finite state machine design, concepts of FSMs, basic design approach, specification methods, state minimization, state encoding, FSM partitioning, implementation of FSMs, programmable logic devices. Elements of computers, arithmetic circuits, arithmetic and logic units, register and bus structures, controllers/ sequencers, microprogramming. Experience with computer-aided design tools for logic design, schematic entry, state diagram entry, hardware description language entry, compilation to logic networks, simulation, mapping to programmable logic devices. Practical topics, non-gate logic, asynchronous inputs and metastability, memories: RAM and ROM, Implementation technologies and mapping problems expressed in words to digital abstractions.

Course Aims

Digital systems are an integral part of many areas of engineering and technology such as personal computers, digital signal processing, telecommunications, speech analysis and recognition and control systems. The objectives of this course are to provide students with the necessary fundamental skills to design and analyze digital circuits in the real world. At the completion of the course, students should be in a position to be able to design and build reliable and cost-effective digital systems.

Course Learning Outcomes

After successfully completing this course, you should be able to:

Learning Outcome	EA Stage 1 Competencies
1. Analyse and design combinational circuits	PE1.1, PE1.2, PE1.3, PE1.5, PE2.1, PE2.2
2. Demonstrate a basic understanding of standard digital circuit elements such as multiplexers, decoders, etc.	PE1.1, PE1.2, PE1.3, PE1.5, PE2.1, PE2.2
3. Design and optimize simple synchronous sequential circuits	PE1.1, PE1.2, PE1.3, PE1.5, PE2.1, PE2.2
4. Understand the fundamentals of the central processing unit (CPU) in a computer	PE1.1, PE1.2, PE1.3, PE1.5, PE2.1, PE2.2
5. Demonstrate knowledge in practical aspects of digital circuits and systems, and their use in more complex systems	PE1.1, PE1.2, PE1.3, PE1.5, PE2.1, PE2.2, PE3.2, PE3.3, PE3.4, PE3.6

Learning Outcome	EA Stage 1 Competencies
6. Demonstrate understanding of the various hardware realizations of the basic digital circuit elements	PE1.1, PE1.2, PE1.3, PE1.5, PE2.1, PE2.2, PE3.2, PE3.3, PE3.4, PE3.6
7. Demonstrate basic skills in working with computer-aided design tools, including knowing the rudiments of a hardware description language (Verilog)	PE1.1, PE1.2, PE1.3, PE1.5, PE2.1, PE2.2
8. Implement simple designs at various levels, from discrete components to programmable logic devices	PE1.3, PE1.5, PE2.1, PE2.2, PE3.2, PE3.4, PE3.6

Teaching Strategies

Delivery Mode

The teaching in this course aims at establishing a good fundamental understanding of the areas covered using:

- Online pre-recorded video lectures, which provide you with a focus on the core analytical material in the course, together with qualitative, alternative explanations to aid your understanding;
- Discussion sessions, which provide you with the opportunity to engage with the lecturer, discuss material presented in the recorded lectures and ask questions to clarify any doubts;
- Workshops, which allow for exercises in problem solving and time for you to resolve problems in understanding lecture material;
- Laboratory sessions, which support the formal lecture material and also provide you with practical construction, measurement and debugging skills.

Learning in this course

You are expected to attend all discussion sessions, workshops, labs, and the mid-term exam in order to maximise learning. You must prepare well for your laboratory classes and your lab work will be assessed. In addition to the lecture notes/video, you should read relevant sections of the recommended text. Reading additional texts will further enhance your learning experience. Group learning is also encouraged. UNSW *assumes* that self-directed study of this kind is undertaken in addition to attending formal classes throughout the course.

Pre-recorded video lecture recordings

The lectures form the core of this subject. Topics presented in lectures will generally be followed by detailed examples to provide students with the real-life applications. Detailed explanations of the topics will be available to students in the form of lecture notes and the prescribed textbook.

Discussion sessions

Discussion sessions will be held in the scheduled lecture times where the key material and examples presented in the lecture videos will be revised and problems solved in a group setting. Students will also be provided the opportunity to ask questions about concepts that need clarification.

Workshops

The workshops are interactive sessions aimed at reinforcing concepts and skills covered in the lectures through problem solving tasks and assessments.

Laboratory sessions

The laboratory schedule is deliberately designed to provide practical, hands-on exposure to the concepts conveyed in lectures. Each week a new design problem is presented. Students will be required to step through the problem to a complete solution using the guidelines given as per lab exercise. The laboratory exercises cover a wide scope ranging from using breadboards and discrete IC components to using industry-standard design software and FPGA implementation. The exercise will follow similar (although simplified) design procedures used in industry.

Additional Course Information

Workload

The expected workload is 15 hours per week throughout the 10-week term.

Relationship to Other Courses

This is a 2nd year course in the School of Electrical Engineering & Telecommunications. It is a core course for students in a BE (Electrical) or (Telecommunications) or (Quantum) program.

Pre-requisites and Assumed Knowledge

The co-requisite for this course is ELEC1111: Electrical Circuit Fundamentals, which introduced basic concepts of electrical circuits. It is assumed that you have a good computer literacy.

Following Courses

The course is a pre-requisite for DESN2000: Engineering Design and Professional Practice, in which the digital system design concepts introduced in ELEC2141 will be applied extensively. It is also a pre-requisite for ELEC3106: Electronics in which low level analysis and implementation of various logic gates are undertaken.

Assessment

The assessment scheme in this course reflects the intention to assess your learning progress through the term. Ongoing assessment occurs through the lab checkpoints (see lab manual), lab exam, mid-term assessments and two assignments. There will be a final cumulative exam at the end of term.

Assessment task	Weight	Due Date	Course Learning Outcomes Assessed
1. Assignments	20%	Not Applicable	1, 2, 3, 5, 6, 7, 8
2. Mid-Term Assessments	25%	Not Applicable	1, 2, 3, 4, 6, 7
3. Final Examination	35%	Not Applicable	1, 2, 3, 4, 6, 7
4. Laboratory practical experiments	20%	Not Applicable	1, 2, 3, 5, 6, 7, 8

Assessment 1: Assignments

The assignments, which will consist of design challenges, form 20% of the overall mark. There will be two assignments for this subject due at the end of week 6 and 9. The assignments will be released at the end of week 2 and week 6, respectively, on Moodle. The assignments will consist of one or more design problems and students are required to provide a complete design solution with verified implementations. All relevant workings, schematic diagrams, HDL codes, and simulations results must be attached to the submissions. All submissions must be made electronically via Moodle. **Assignment 1 is due on March 27 (Monday, Week 7). Assignment 2 is due on April 21 (Friday, Week 10). No late submission will be possible after the due time.**

Though generic guidelines will be provided, there will be no one “correct” solution to the assignments. Students will be expected to work independently on their implementation and to be able to justify the unique design choices along the way.

This is not a Turnitin assignment

Assessment 2: Mid-Term Assessments

The midterm assessment has two parts: weekly quizzes worth 10% and a mid-term exam in week 5 worth 15%.

1. Weekly Workshop Quizzes

There will be weekly quizzes in each of the workshops throughout the term. The purpose of the quizzes is to keep students up to date with the lecture material and to test understanding of the course concepts. These quizzes will make up 10% of the overall mark. Each quiz will consist of a number of randomly selected questions from a pool of questions so that students may not have exactly the same set of questions. The quiz will be marked according to the number of correct answers. The quizzes are a mandatory component of the overall assessment and failure to attempt a quiz will result in no marks being given for the quiz. Each quiz will only be available during the workshop. No late attempts will be permitted. **Quizzes should be attempted genuinely and independently. If Moodle suspects**

dependent and insincere practices, it will alert the course convener.

2. Mid-Term Exam

The midterm exam in this course is an online 1-hour examination, comprising two compulsory questions. It accounts for 15% of the overall mark. University approved calculators are allowed. The examination tests analytical and critical thinking and general understanding of the course material in a controlled fashion. Questions will be drawn from the topics covered in the first four weeks of the course, unless specifically indicated otherwise by the lecturer. Marks will be assigned according to the correctness of the responses. The exam will be held will be held in the week of March 13, 2023 during the week 5 worskhops.

Assessment 3: Final Examination

The exam in this course is a two-hour cumulative written examination, comprising four compulsory questions. It accounts for 35% of the overall mark. University approved calculators are allowed. The examination tests analytical and critical thinking and general understanding of the course material in a controlled fashion. Questions may be drawn from any aspect of the course (including laboratory), unless specifically indicated otherwise by the lecturer. Marks will be assigned according to the correctness of the responses.

Assessment 4: Laboratory practical experiments (Group)

The laboratory experiments will be assessed in two parts: weekly laboratory assessments worth 15% in total and a final lab exam in week 10 worth 5%.

1. Laboratory Assessment

Laboratories are primarily about learning, and the laboratory assessment is designed mainly to check your knowledge as you progress through each stage of the laboratory tasks. It is essential that you complete the laboratory preparation before coming to the lab. **This includes reading over each lab in the lab manual and completing the pre-lab quiz on Moodle before each session. Students will not be allowed to start the lab unless they have answered all the questions in the pre-lab quiz. Students will have unlimited attempts to complete the pre-lab quiz.** Each lab exercise will have one check point that will be marked by the laboratory demonstrators. Although there is only one check point for each lab, there are several results that students are required to demonstrate when marked for the check point. Therefore, you are strongly advised to (i) record results on the lab manual; (ii) save the accomplished tasks or results on working directory in the lab PC; (iii) keep the working circuit on the breadboard for the laboratory demonstrators to check. Laboratory demonstrators will be available to help students with any questions or difficulties.

Upon completion of a checkpoint, students will be required to write down their student and bench numbers on the Laboratory Queue Sheet and wait for the laboratory assessor to mark their work. Students may continue working on subsequent lab tasks while waiting to be assessed. Students will be required to show the working of their task for each checkpoint and answer questions asked by the laboratory assessor to demonstrate their understanding of the ideas addressed within each task.

Students will work in pairs but be marked individually. Each student will be asked a few questions. There will also be a mark for the group based on demonstrating the required lab tasks. Refer to the laboratory manual for the marking guideline.

Assessment marks will be awarded according to your preparation (completing set preparation exercises and correctness of these or readiness for the lab in terms of pre-reading), how much of the lab you were able to complete, your understanding of the experiments conducted during the lab, the quality of the code you write during your lab work (according to the guidelines given in lectures), and your understanding of the topic covered by the lab.

After completing each experiment, your work will be assessed by the laboratory demonstrator. Both the results sheet and your lab book will be assessed by the laboratory demonstrator.

2. Laboratory Exam

To check that you have achieved the practical learning outcomes for the course, you will be examined in the laboratory. Laboratory Exams are closed book practical exams that will assess your technical understanding of using design software tools used throughout the labs in simulating, verifying, and implementing digital circuits on the FPGA board. You will be given two design problems, asked to implement and verify the design on the FPGA board. Marks will be awarded for the correct understanding of practical and relevant theoretical concepts, correct operation of laboratory equipment, and correct interpretation of measured results.

Attendance Requirements

Students are strongly encouraged to attend all classes and review lecture recordings.

Course Schedule

View class timetable

Timetable

Date	Type	Content
Week 1: 13 February - 17 February	Topic	Introduction to digital systems, number systems & combinational logic circuits
Week 2: 20 February - 24 February	Topic	Combinational logic circuit analysis
	Laboratory	Introduction to digital circuits
Week 3: 27 February - 3 March	Topic	Combinational logic circuit design
	Laboratory	Xilinx ISE and Digilent Nexys 3
Week 4: 6 March - 10 March	Topic	Combinational circuit blocks & arithmetic circuits
	Laboratory	Comprehensive Guide to FPGA Programming
Week 5: 13 March - 17 March	Topic	Midterm exam
	Laboratory	Combinational circuit design
	Assessment	Mid-term exam (March 13, 4-5 pm)
Week 7: 27 March - 31 March	Topic	Sequential circuit elements and analysis
	Laboratory	Flip-Flop basics
	Assessment	Assignment 1 due (March 27)
Week 8: 3 April - 7 April	Topic	Sequential circuit design
	Laboratory	Sequential circuit design
Week 9: 10 April - 14 April	Topic	Registers and computer design fundamentals
	Laboratory	Addressable RGB LED Controller Design
Week 10: 17 April - 21 April	Topic	Digital logic families and CMOS technology
	Laboratory	Lab exam
	Assessment	Assignment 2 due (April 21)

Resources

Prescribed Resources

M. Mano, C. R. Kime and T. Martin, Logic and Computer Design Fundamentals, 5th Edition (Global Edition), Pearson, 2016.

Recommended Resources

M. Mano, C. R. Kime, Logic and Computer Design Fundamentals, 4th Edition, Prentice Hall, 2008

R. H. Katz & G. Borriello, Contemporary Logic Design, 2nd Edition, Prentice Hall, 2005

M. Mano & M. D. Cilietti, Digital Design, 4th Edition, Prentice Hall, 2007

J. F. Wakerly, Digital Design: Principles and Practices, 4th Edition, Prentice Hall, 2006

Course Evaluation and Development

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the online student survey myExperience. You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings. As a result of previous feedback obtained for this course and in our efforts to provide a rich and meaningful learning experience, we have continued to evaluate and modify our delivery and assessment methods.

More time will be spent in the lectures on Verilog and CMOS technology. The students use the online lecture recordings extensively so more details recordings will be created to better support their learning. Additional problem solving videos have been created and will be provided to the students.

Laboratory Workshop Information

Workshops

Workshops will be held in Weeks 1 to 10. You should attempt all of the questions in the workshop sheet posted on Moodle in advance of attending the workshops. The importance of adequate preparation prior to each workshop cannot be overemphasized, as the effectiveness and usefulness of the workshop depends to a large extent on this preparation. Group learning is encouraged. Answers for these questions will be discussed during the workshop and the tutor will cover the more complex questions in the workshop. In addition, during the workshop, you will be quizzed individually on similar but new questions which will be marked and count towards your final mark. Solutions to the workshop questions and videos explaining the solutions will be posted on Moodle at the end of the week.

Laboratory program

Laboratories will be held in Weeks 2 to 10. The laboratory schedule is deliberately designed to provide practical, hands-on exposure to the concepts conveyed in lectures. Each week a new design problem is presented. Students will be required to step through the problem to a complete solution using the guidelines given as per lab exercise. The laboratory exercises cover a wide scope ranging from using breadboards and discrete IC components to using industry-standard design software and FPGA

implementation. The exercise will follow similar (although simplified) design procedures used in industry.

The laboratory manual will be uploaded on Moodle. Every student will need to bring a lab pack with them to the lab, that can be ordered online from https://recharge.it.unsw.edu.au, prior to attending the first laboratory class. The lab pack will contain all hardware components you will need for the entire lab. Without the hardware components in the lab pack, you will not be able to do some of the laboratory activities and therefore it is important you bring you lab pack to the laboratory class. You will also need to bring the breadboards previously used in ELEC1111 to the laboratory. Breadboards will also be offered for sale through the school office.

Laboratory attendance WILL be kept, and you MUST attend at least 80% of the labs. Prior to attending each lab, you must read over each lab in the lab manual and complete the pre-lab quiz on Moodle before each session. You will not be allowed to start the lab unless you have answered all the questions in the pre-lab quiz.

A broad understanding of the tools utilized in these exercises is highly encouraged and a bonus lab task will be available to students after the successful completion of all other exercises. The bonus task will carry on from the last lab exercise and will be accompanied by minimal guidelines, allowing students to further demonstrate their ability to analyse and resolve issues independently. The optional labs should be done under minimal supervision and only considered or marked after the student has finished all mandatory labs.

More details of the online laboratory plan for the online laboratory session will be announced through Moodle announcements in Week 1.

Laboratory Exemption

There is no laboratory exemption for this course. Regardless of whether equivalent labs have been completed in previous courses, all students enrolled in this course must take the labs. If, for medical reasons, (note that a valid medical certificate must be provided) you are unable to attend a lab, you will need to apply for a catch-up lab during another lab time or in the online lab, as agreed by the laboratory coordinator.

Academic Honesty and Plagiarism

Academic Honesty and Plagiarism

Plagiarism is the unacknowledged use of other people's work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a form of academic misconduct, and the University has very strict rules that include some severe penalties. For UNSW policies, penalties and information to help you avoid plagiarism, see https://student.unsw.edu.au/plagiarism. To find out if you understand plagiarism correctly, try this short quiz: https://student.unsw.edu.au/plagiarism-quiz.

General Conduct and Behaviour

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and students may be asked to leave the class.

Academic Information

COVID19 - Important Health Related Notice

Your health and the health of those in your class is critically important. You must stay at home if you are sick or have been advised to self-isolate by NSW health or government authorities. **You will not be penalised for missing a face-to-face activity due to illness or a requirement to self-isolate**. We will work with you to ensure continuity of learning during your isolation and have plans in place for you to catch up on any content or learning activities you may miss. Where this might not be possible, an application for fee remission may be discussed.

If you are required to self-isolate and/or need emotional or financial support, please contact the Nucleus: Student Hub. If you are unable to complete an assessment, or attend a class with an attendance or participation requirement, please let your teacher know and apply for special consideration through the Special Consideration portal. To advise the University of a positive COVID-19 test result or if you suspect you have COVID-19 and are being tested, please fill in this form.

UNSW requires all staff and students to follow NSW Health advice. Any failure to act in accordance with that advice may amount to a breach of the Student Code of Conduct. Please refer to the Safe Return to Campus guide for students for more information on safe practices.

Dates to note

Important Dates available at: https://student.unsw.edu.au/dates

Student Responsibilities and Conduct

Students are expected to be familiar with and adhere to all UNSW policies (see https://student.unsw.edu.au/policy), and particular attention is drawn to the following:

Workload

It is expected that you will spend at least **15 hours per week** studying a 6 UoC course, from Week 1 until the final assessment, including both formal classes and *independent, self-directed study*. In periods where you need to complete assignments or prepare for examinations, the workload may be greater. Over-commitment has been a common source of failure for many students. You should take the required workload into account when planning how to balance study with employment and other activities.

Attendance

Regular and punctual attendance at all classes is expected. UNSW regulations state that if students attend less than 80% of scheduled classes they may be refused final assessment.

Work Health and Safety

UNSW policy requires each person to work safely and responsibly, in order to avoid personal injury and to protect the safety of others.

Special Consideration and Supplementary Examinations

You must submit all assignments and attend all examinations scheduled for your course. You can apply for special consideration when illness or other circumstances beyond your control interfere with an assessment performance. If you need to submit an application for special consideration for an exam or assessment, you must submit the application **prior to the start** of the exam or before the assessment is submitted, except where illness or misadventure prevent you from doing so. Be aware of the "fit to sit/submit" rule which means that if you sit an exam or submit an assignment, you are declaring yourself well enough to do so and cannot later apply for Special Consideration. For more information and how to apply, see https://student.unsw.edu.au/special-consideration.

Administrative Matters

On issues and procedures regarding such matters as special needs, equity and diversity, occupational health and safety, enrolment, rights, and general expectations of students, please refer to the School and UNSW policies:

https://student.unsw.edu.au/guide

https://www.unsw.edu.au/engineering/our-schools/electrical-engineering-telecommunications/student-life/resources

Disclaimer

This Course Outline sets out description of classes at the date the Course Outline is published. The nature of classes may change during the Term after the Course Outline is published. Moodle should be consulted for the up-to-date class descriptions. If there is any inconsistency in the description of activities between the University timetable and the Course Outline (as updated in Moodle), the description in the Course Outline/Moodle applies.

Image Credit

https://wallpaperaccess.com/blue-motherboard

CRICOS

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Acknowledgement of Country

We acknowledge the Bedegal people who are the traditional custodians of the lands on which UNSW Kensington campus is located.

Appendix: Engineers Australia (EA) Professional Engineer Competency Standard

Program Intended Learning Outcomes	
Knowledge and skill base	
PE1.1 Comprehensive, theory based understanding of the underpinning natural and physical sciences and the engineering fundamentals applicable to the engineering discipline	✓
PE1.2 Conceptual understanding of the mathematics, numerical analysis, statistics, and computer and information sciences which underpin the engineering discipline	✓
PE1.3 In-depth understanding of specialist bodies of knowledge within the engineering discipline	✓
PE1.4 Discernment of knowledge development and research directions within the engineering discipline	
PE1.5 Knowledge of engineering design practice and contextual factors impacting the engineering discipline	✓
PE1.6 Understanding of the scope, principles, norms, accountabilities and bounds of sustainable engineering practice in the specific discipline	
Engineering application ability	
PE2.1 Application of established engineering methods to complex engineering problem solving	✓
PE2.2 Fluent application of engineering techniques, tools and resources	✓
PE2.3 Application of systematic engineering synthesis and design processes	
PE2.4 Application of systematic approaches to the conduct and management of engineering projects	
Professional and personal attributes	
PE3.1 Ethical conduct and professional accountability	
PE3.2 Effective oral and written communication in professional and lay domains	✓
PE3.3 Creative, innovative and pro-active demeanour	✓
PE3.4 Professional use and management of information	✓
PE3.5 Orderly management of self, and professional conduct	
PE3.6 Effective team membership and team leadership	✓