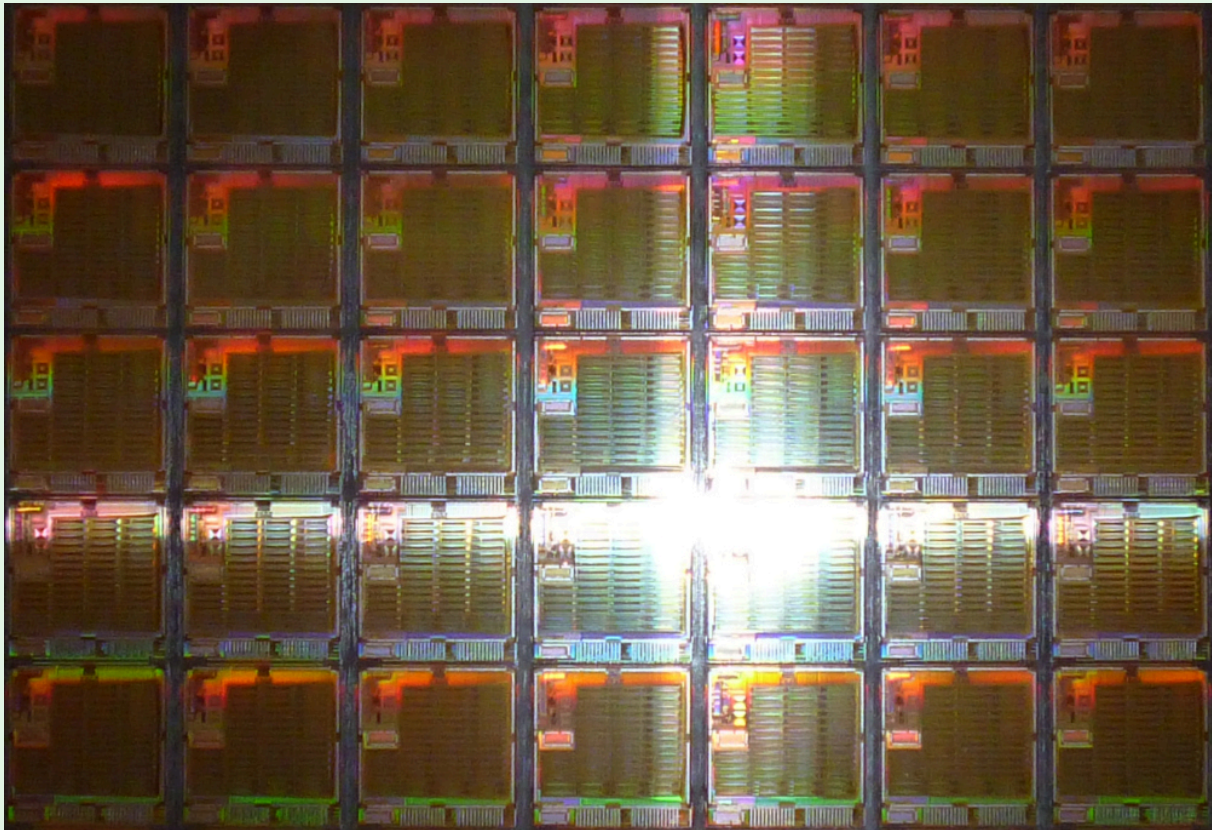


ELEC4602

Microelectronic Design and Technology

Term 3, 2022



Course Overview

Staff Contact Details

Convenors

Name	Email	Availability	Location	Phone
Torsten Lehmann	t.lehmann@unsw.edu.au	Tuesdays 12-1pm, Thursdays 4-5pm	G17-343	93855374

Tutors

Name	Email	Availability	Location	Phone
Julian Keledjian	julian.keledjian@unsw.edu.au			

School Contact Information

Consultations: Lecturer consultation times will be advised during the first lecture. You are welcome to email the tutor or laboratory demonstrator, who can answer your questions on this course and can also provide you with consultation times. ALL email enquiries should be made from your student email address with ELEC/TELExxxx in the subject line; otherwise they will not be answered.

Keeping Informed: Announcements may be made during classes, via email (to your student email address) and/or via online learning and teaching platforms – in this course, we will use Moodle <https://moodle.telt.unsw.edu.au/login/index.php>. Please note that you will be deemed to have received this information, so you should take careful note of all announcements.

Student Support Enquiries

[For enrolment and progression enquiries please contact Student Services](#)

Web

[Electrical Engineering Homepage](#)

[Engineering Student Support Services](#)

[Engineering Industrial Training](#)

[UNSW Study Abroad and Exchange](#) (for inbound students)

[UNSW Future Students](#)

Phone

(+61 2) 9385 8500 – Nucleus Student Hub

(+61 2) 9385 7661 – Engineering Industrial Training

(+61 2) 9385 3179 – UNSW Study Abroad and UNSW Exchange (for inbound students)

Email

[Engineering Student Support Services](#) – current student enquiries

- e.g. enrolment, progression, clash requests, course issues or program-related queries

[Engineering Industrial Training](#) – Industrial training questions

[UNSW Study Abroad](#) – study abroad student enquiries (for inbound students)

[UNSW Exchange](#) – student exchange enquiries (for inbound students)

[UNSW Future Students](#) – potential student enquiries

- e.g. admissions, fees, programs, credit transfer

Course Details

Units of Credit 6

Summary of the Course

Basic IC processing technology: lithography, oxidation, diffusion, implantation, film deposition, etching, metalisation. IC layout, layout layers and functions, design rules, scaling. Design synthesis and verification tools, p-cells, cell libraries, place-and-route, HDL compilers, layout-versus-schematic, circuit simulators. Analogue and digital MOS device models. On-chip components: capacitors, inductors, resistors, diodes. Floor planing, cell layout and routing. Corner and Monto Carlo simulations. CMOS analogue building blocks: current mirrors, differential stage, active load, single-stage amplifiers. Noise sources and analysis. CMOS operational amplifier design, frequency compensation, output stages. D/A converters and A/D converters. Ring oscillators. Static CMOS gates and flip-flops, transmission gates. CMOS digital building blocks: level shifters, decoders, multiplexers, tri-states, buffers. Gate timing. Memories: ROM, SRAM and DRAM cell design; sense amplifiers.

Course Aims

Background

Microelectronics or integrated electronics is the miniaturised electronic circuits that make up Integrated Circuits (ICs) such as microprocessors, Field-Programmable Gate Arrays, Flash-memories, operational amplifier, analogue-to-digital converters and many other functions. Most ICs today are implemented in various flavours of CMOS technology which is the focus of this course. The ability to use large number of components at relative low cost and the ability to match components accurately on-chip makes the design of integrated circuits and systems different from a similar design using discrete components. Microelectronics Design and Technology is a broad based, introductory IC design course, which takes the student through all the necessary steps in order to complete (ready-to-manufacture) a basic mixed-signal front-end in a typical integrated system.

Aims

The course aims to make the student familiar with CMOS microelectronics technologies, and enable the student to do analysis and design of circuits implemented in these technologies.

Course Learning Outcomes

After successfully completing this course, you should be able to:

Learning Outcome	EA Stage 1 Competencies
1. Appreciate capabilities and limitations of current microelectronic (or IC) technologies	PE1.3, PE1.4
2. Use modern CAD design tools to design ICs	PE1.3, PE1.5, PE2.2, PE3.2
3. Create IC layouts	PE1.3, PE1.5, PE2.1, PE2.2, PE2.3, PE3.2
4. Understand and use circuit models of IC components	PE1.2, PE1.3, PE1.5

Learning Outcome	EA Stage 1 Competencies
5. Analyse simple analogue and digital microelectronic circuits	PE1.1, PE1.2, PE1.3, PE1.5, PE2.1, PE2.2, PE2.3
6. Design simple analogue, digital and mixed microelectronic circuits	PE1.3, PE1.5, PE2.1, PE2.2, PE2.3, PE3.2, PE3.3, PE3.4, PE3.5

Targeted Graduate Capabilities

Electrical Engineering and Telecommunications programs are designed to address the following targeted capabilities which were developed by the school in conjunction with the requirements of professional and industry bodies:

- The ability to apply knowledge of basic science and fundamental technologies;
- The skills to communicate effectively, not only with engineers but also with the wider community;
- The capability to undertake challenging analysis and design problems and find optimal solutions;
- Expertise in decomposing a problem into its constituent parts, and in defining the scope of each part;
- A working knowledge of how to locate required information and use information resources to their maximum advantage;
- Proficiency in developing and implementing project plans, investigating alternative solutions, and critically evaluating differing strategies;
- An understanding of the social, cultural and global responsibilities of the professional engineer;
- The ability to work effectively as an individual or in a team;
- An understanding of professional and ethical responsibilities;
- The ability to engage in lifelong independent and reflective learning.

UNSW Graduate Capabilities

The course delivery methods and course content directly or indirectly addresses a number of core UNSW graduate capabilities, as follows:

- Developing rigorous analysis, critique, and reflection, and ability to apply knowledge and skills to solving problems, through laboratory experiments and tutorial exercises.
- Developing capable independent and collaborative enquiry, through tutorials exercises.
- Developing digital and information literacy and lifelong learning skills, through lectures, class preparations and report writing.
- Developing the capability of effective communication, through report writing.
- Developing independent, self-directed professionals who are enterprising, innovative, creative and responsive to change, through the design task.

Teaching Strategies

Delivery Mode

- Lecture recordings and following Q&A sessions, which provide you with a focus on the core analytical material in the course, together with qualitative, alternative explanations and individually targeted illustrations to aid your understanding;
- Self-guided tutorials, which allow for exercises in problem solving and allow time for you to resolve in-depth problems for quantitative understanding of the lecture material;

- Computer laboratory sessions, which support, via detailed simulations using state-of-the-art CAD tools, the formal lecture material and also provide you with practical design, and debugging skills;
- A design task, which draws together theoretical and practical design aspects in an open-ended realistic design problem, reinforcing the course material.

Learning in this Course

You are expected to watch all lecture recordings and attend all Q&A sessions, labs, and quizzes, as well as completing the tutorials, in order to maximise your learning. You must prepare well for your laboratory classes and your lab work will be assessed. You should read relevant sections of the recommended texts. For most topics, lecture notes will not be given: reading and reflecting on the recommended texts and identify critical parts with the aid of the lectures is an essential component of this course. Reading additional texts will further enhance your learning experience. Group learning is also encouraged. UNSW assumes that self-directed study of this kind is undertaken in addition to attending face-to-face classes throughout the course.

Lecture recordings and Q&A sessions

During the lecture recordings technology capabilities and design issues are discussed and theoretical aspects of IC design and technology are presented. Numerous examples of analogue and digital integrated circuit functions are discussed in order to convey a qualitative understanding of circuit operations. You are encouraged to actively engage in the Q&A sessions to facilitate two-way communication and enhance learning. The lecture recordings and Q&A sessions aim to support you in analysing and designing integrated circuits, and to help you appreciate the capabilities of IC technologies.

Self-guided tutorials

You should attempt all of your problem sheet questions as indicated in the tutorial schedule. Group learning is encouraged. Answers for these questions may be discussed during the consultation time or at some other agreed-upon time.

Laboratory Program

The laboratory work provides you with hands-on design experience and exposure to state-of-the-art CAD tools. The laboratory thus enables you to use these tools for IC circuit design, analysis and lay-out, and re-enforces the central topics in the course. Verifying circuit functions by simulations also train you in best-practice IC verification and exercises your ability to locate circuit errors.

Design Task

The design task aims to draw together theoretical and practical design aspects in an open-ended realistic design problem. You will design an integrated circuit meeting given specifications, use the CAD tools to verify the circuit operation and write a report documenting your design. The design task provide and test engineering creativity, open-ended problem solving skills, communication skills and general understanding of the course content. You may use the CAD tools in rooms G17-202/G17-209/G17-217 for this task. You may also use up to 1 h/week of the scheduled laboratory time for the design task where demonstrators can assist you.

Additional Course Information

Relationship to Other Courses

This is a 4th year course in the School of Electrical Engineering and Telecommunications. It is a professional elective course for students following a BE (Electrical) or (Telecommunications) program and other combined degree programs.

Pre-requisites and Assumed Knowledge

The pre-requisite for this course is ELEC3106, Electronics. It is essential that you have good working knowledge of circuit theory, basic analogue and digital electronics, and basic signal analysis as covered in the courses ELEC1112, Electrical Circuits, ELEC2133, Analogue Electronics, ELEC2141, Digital Circuit Design, and ELEC2134, Circuits and Signals. It is finally assumed that you are proficient in the use of personal computers.

Following Courses

The course is a co-requisite for the post-graduate course ELEC9701, Mixed Signal Microelectronics Design. The course is also a co-requisite for thesis work in the area of integrated circuit design.

Assessment

Assessment task	Weight	Due Date	Course Learning Outcomes Assessed
1. Laboratory work	15%		1, 2, 3
2. Quizzes	10%		4, 5
3. Design task	15%		1, 2, 4, 6
4. Final examination	60%		1, 3, 4, 5, 6

Assessment 1: Laboratory work

Submission notes: See Moodle for laboratory report submission dates.

Deadline for absolute fail: Five days after each laboratory report submission deadline.

While laboratory work is primarily about learning, it is assessed to ensure that you understand the material in this essential course component. This assessment test that you can use the CAD tools, create IC layouts, understand circuit models and functions, carry out appropriate simulations, and can design simple circuits.

You are required to maintain a lab book for recording your observations and you must bring a USB stick (or have cloud storage access) to capture screen shots or print-outs of your work for documentation. After completing each key lab component, your work will be assessed by the laboratory demonstrator, so make sure that your demonstrator notice your work. Laboratory work must be documented in brief reports which are due Monday the week after the laboratory session ending each exercise. Late submissions carry a 5% penalty per day and will not be accepted beyond five days delay. Delays on medical grounds are accepted. Each report must be uploaded as a .pdf file (no other format accepted) on the course Moodle site.

Assessment criteria

Assessment marks (grade only) will be awarded according to how much of the lab you were able to complete, your understanding of the work conducted during the lab, and your ability to concisely express lab findings in your report. A HD mark is given only for exceptional performance that includes an attempt to complete any laboratory extensions; a serious attempt at completing the problems is required for a PS mark.

Assessment 2: Quizzes

Submission notes: See Moodle for quiz dates and times.

There are two quizzes held during the lecture time through the term. These are designed to give early feedback on your progress through the theoretical components of the course and test your general understanding of the course material. Questions will be drawn from course material covered in the three weeks prior to each quiz.

Assessment criteria

Assessment marks are given according to the correct fraction of the answers to the quiz questions.

Assessment 3: Design task

Submission notes: See Moodle for design report submission date.

Deadline for absolute fail: Five days after the design report submission deadline.

The design task is assessed to test your ability to design a simple integrated circuit, thus also demonstrating your appreciation of the technology, your ability to use appropriate models and simulations, and your ability to conduct suitable analysis to aid in the design. As for the other laboratory work, you should maintain a lab book and must record suitable screen shots or print-outs as documentation for your work. The design and verification work must be documented in a brief report which is due Monday the due week listed in the laboratory schedule. Late submissions carry a 5% penalty per day and will not be accepted beyond five days delay. Delays on medical grounds are accepted. Each report must be uploaded as a .pdf file (no other format accepted) on the course Moodle site.

Assessment criteria

Assessment marks (grade only) will be awarded on the basis of your report according to your understanding of the design problem, simulations carried out, the quality and innovativeness of your design, and your ability to concisely explain and characterise your design in your report. A HD mark is given only for exceptional performance that exceed design requirements; a serious attempt at completing the problem is required for a PS mark.

Assessment 4: Final examination

The exam in this course is an open-book 2 hour (nominal) written examination. University approved calculators are allowed. The examination tests analytical and critical thinking and general understanding of the course material in a controlled fashion. Questions may be drawn from any aspect of the course (including laboratories and design task), unless specifically indicated otherwise by the lecturer.

Assessment criteria

Assessment marks will be assigned according to the correctness of the responses.

Hurdle requirement

An examination mark of at least 45% is required to pass the course.

Attendance Requirements

Students are strongly encouraged to attend all classes and review lecture recordings.

Course Schedule

[View class timetable](#)

Timetable

Date	Type	Content
Week 1: 12 September - 16 September	Lecture	CMOS processing technologies and components. Layout layers.IC layout and design rules.
	Reading	JB ch. 7, web, JB ch. 3, 4, 5.
	Laboratory	Lab 1: layout.
	Tutorial	Tute 1: layout.
Week 2: 19 September - 23 September	Lecture	Design Synthesis and verification tools. Analogue MOS models.
	Reading	Web. JB ch. 9.
	Laboratory	Lab 1 continued.
	Tutorial	Tute 2: transistor models.
Week 3: 26 September - 30 September	Lecture	Digital MOS models and device noise. Current mirrors.
	Reading	JB ch. 10, JB ch. 8, JB ch. 20.
	Laboratory	Lab 2: circuit simulation.
	Tutorial	Tute 3: single-stage amplifiers.
	Assessment	Lab 1 report due.
Week 4: 3 October - 7 October	Lecture	Single-stage amplifiers. Operational amplifier design I.
	Reading	JB ch. 21, 22.
	Laboratory	Lab 3: op-amp design.
	Tutorial	Tute 4: op-amps.
	Assessment	Lab 2 report due.
	Assessment	Quiz 1.
Week 5: 10 October -	Lecture	Operational amplifier design II. Comparators.

14 October		Charge Injection.
	Reading	JB ch. 24, 27, JB ch. 25.
	Laboratory	Lab 3 continued.
	Tutorial	Tute 5: sampling and comparators.
	Project	Design task.
Week 6: 17 October - 21 October	Project	Design task.
Week 7: 24 October - 28 October	Lecture	Samplers, data converter metrics, D/A and A/D converter design.
	Reading	JB ch. 25, 28, 29.
	Laboratory	Lab 4: combinational logic.
	Tutorial	Tute 6: A/D converters.
	Assessment	Lab 3 report due.
	Project	Design task.
Week 8: 31 October - 4 November	Lecture	CMOS inverters and logic. Buffers and sizing.
	Reading	JB ch. 11.
	Laboratory	Lab 4 continued.
	Tutorial	Tute 7: CMOS inverters.
	Assessment	Quiz 2.
	Project	Design task.
Week 9: 7 November - 11 November	Lecture	Static CMOS logic design. Sequential CMOS logic.
	Reading	JB ch. 12, 13.
	Laboratory	Lab 5: sequential logic.
	Tutorial	Tute 8: CMOS logic.
	Assessment	Lab 4 report due.
	Project	Design task.
Week 10: 14 November - 18 November	Lecture	Dynamic CMOS logic. Memory design and topologies.
	Reading	JB ch. 14, 16.
	Laboratory	Lab 5 continued.

	Tutorial	Tute 9: sequential logic.
	Assessment	Design task report due.
Study Week: 21 November - 24 November	Assessment	Lab 5 report due.

Resources

Prescribed Resources

Textbook

- R. J. Baker, CMOS Circuit Design, Layout, and Simulation. Wiley Interscience, 3rd/4th ed., 2010/2019.

On-line resources

Moodle: As a part of the teaching component, Moodle will be used to upload lab reports and host forums. Assessment marks will also be made available via Moodle:

<https://moodle.telt.unsw.edu.au/login/index.php>.

Course webpage: The course webpage is used to disseminate course material, including laboratory notes and design brief, past assessment and examination papers, and some lecture notes:

<https://subjects.ee.unsw.edu.au/elec4602>.

Teams: Teams (accessed using your University zpass credentials) will be used for on-line real-time communications. Q&A sessions will be accessible via Teams and students doing laboratory classes remotely will need to use Teams to communicate with their laboratory demonstrator during classes:

<https://teams.microsoft.com/>.

CAD resources

Students will use the PCs in the Signal Processing Laboratory G17-108 for all in-class laboratory work. The CAD tools used in this course is the industry standard Cadence design suite which run under the Linux system Virtual Machine on the lab PCs. For specific details on how to log on, see the course web page. Students can access the CAD tools on the PCs in the school located in rooms G17-202 and G17-217 as well as the open space area G17-209.

Remote computer access

Computers in rooms G17-202 and G17-217 can be accessed remotely via <https://aaa-access.unsw.edu.au/vpn/index.html>. Click on DESKTOPS and subsequently ELECENG-LABPC-G17-Rm202 or ELECENG-LABPC-G17-Rm217 to start a Citrix remote session on a computer in one of those rooms. Students must have the Citrix Workspace player (download from <https://www.citrix.com/en-au/downloads/workspace-app/>) installed on their own computer.

Recommended Resources

Reference books

- T. C. Carusone, D. A. Johns and K. W. Martin, Analog Integrated Circuit Design. Wiley and Sons Inc., 2nd ed., 2012.
- T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits. Cambridge University Press, 1998.
- N. Weste and D. Harris, CMOS VLSI Design: a Circuits and Systems Perspective. Addison-Wesley, 3rd ed., 2005

Course Evaluation and Development

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the Course and Teaching Evaluation and Improvement Process. You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings. As a result of previous feedback obtained for this course, and in our efforts to provide a rich and meaningful learning experience, we have changed the weighting of in-term assessments, introduced formal tutorial classes, and released summary slides.

Academic Honesty and Plagiarism

Academic Honesty and Plagiarism

Plagiarism is the unacknowledged use of other people's work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a form of academic misconduct, and the University has very strict rules that include some severe penalties. For UNSW policies, penalties and information to help you avoid plagiarism, see <https://student.unsw.edu.au/plagiarism>. To find out if you understand plagiarism correctly, try this short quiz: <https://student.unsw.edu.au/plagiarism-quiz>.

General Conduct and Behaviour

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and students may be asked to leave the class.

Academic Information

COVID19 - Important Health Related Notice

Your health and the health of those in your class is critically important. You must stay at home if you are sick or have been advised to self-isolate by [NSW health](#) or government authorities. Current alerts and a list of hotspots can be found [here](#). **You will not be penalised for missing a face-to-face activity due to illness or a requirement to self-isolate.** We will work with you to ensure continuity of learning during your isolation and have plans in place for you to catch up on any content or learning activities you may miss. Where this might not be possible, an application for fee remission may be discussed.

If you are required to self-isolate and/or need emotional or financial support, please contact the [Nucleus: Student Hub](#). If you are unable to complete an assessment, or attend a class with an attendance or participation requirement, please let your teacher know and apply for [special consideration](#) through the [Special Consideration portal](#). To advise the University of a positive COVID-19 test result or if you suspect you have COVID-19 and are being tested, please fill in this [form](#).

UNSW requires all staff and students to follow NSW Health advice. Any failure to act in accordance with that advice may amount to a breach of the Student Code of Conduct. Please refer to the [Safe Return to Campus](#) guide for students for more information on safe practices.

Dates to note

Important Dates available at: <https://student.unsw.edu.au/dates>

Student Responsibilities and Conduct

Students are expected to be familiar with and adhere to all UNSW policies (see <https://student.unsw.edu.au/policy>), and particular attention is drawn to the following:

Workload

It is expected that you will spend at least **15 hours per week** studying a 6 UoC course, from Week 1 until the final assessment, including both formal classes and *independent, self-directed study*. In periods where you need to complete assignments or prepare for examinations, the workload may be greater. Over-commitment has been a common source of failure for many students. You should take the required workload into account when planning how to balance study with employment and other activities.

Attendance

Regular and punctual attendance at all classes is expected. UNSW regulations state that if students attend less than 80% of scheduled classes they may be refused final assessment.

Work Health and Safety

UNSW policy requires each person to work safely and responsibly, in order to avoid personal injury and to protect the safety of others.

Special Consideration and Supplementary Examinations

You must submit all assignments and attend all examinations scheduled for your course. You can apply for special consideration when illness or other circumstances beyond your control interfere with an assessment performance. If you need to submit an application for special consideration for an exam or assessment, you must submit the application **prior to the start** of the exam or before the assessment is submitted, except where illness or misadventure prevent you from doing so. Be aware of the “fit to sit/submit” rule which means that if you sit an exam or submit an assignment, you are declaring yourself well enough to do so and cannot later apply for Special Consideration. For more information and how to apply, see <https://student.unsw.edu.au/special-consideration>.

Administrative Matters

On issues and procedures regarding such matters as special needs, equity and diversity, occupational health and safety, enrolment, rights, and general expectations of students, please refer to the School and UNSW policies:

<https://student.unsw.edu.au/guide>

<https://www.engineering.unsw.edu.au/electrical-engineering/resources>

Disclaimer

This Course Outline sets out description of classes at the date the Course Outline is published. The nature of classes may change during the Term after the Course Outline is published. Moodle should be consulted for the up-to-date class descriptions. If there is any inconsistency in the description of activities between the University timetable and the Course Outline (as updated in Moodle), the description in the Course Outline/Moodle applies.

Image Credit

Close-up of wafer diced into chips (c) 2012 Torsten Lehmann

CRICOS

CRICOS Provider Code: 00098G

Acknowledgement of Country

We acknowledge the Bedegal people who are the traditional custodians of the lands on which UNSW Kensington campus is located.

Appendix: Engineers Australia (EA) Professional Engineer Competency Standard

Program Intended Learning Outcomes	
Knowledge and skill base	
PE1.1 Comprehensive, theory based understanding of the underpinning natural and physical sciences and the engineering fundamentals applicable to the engineering discipline	✓
PE1.2 Conceptual understanding of the mathematics, numerical analysis, statistics, and computer and information sciences which underpin the engineering discipline	✓
PE1.3 In-depth understanding of specialist bodies of knowledge within the engineering discipline	✓
PE1.4 Discernment of knowledge development and research directions within the engineering discipline	✓
PE1.5 Knowledge of engineering design practice and contextual factors impacting the engineering discipline	✓
PE1.6 Understanding of the scope, principles, norms, accountabilities and bounds of sustainable engineering practice in the specific discipline	
Engineering application ability	
PE2.1 Application of established engineering methods to complex engineering problem solving	✓
PE2.2 Fluent application of engineering techniques, tools and resources	✓
PE2.3 Application of systematic engineering synthesis and design processes	✓
PE2.4 Application of systematic approaches to the conduct and management of engineering projects	
Professional and personal attributes	
PE3.1 Ethical conduct and professional accountability	
PE3.2 Effective oral and written communication in professional and lay domains	✓
PE3.3 Creative, innovative and pro-active demeanour	✓
PE3.4 Professional use and management of information	✓
PE3.5 Orderly management of self, and professional conduct	✓
PE3.6 Effective team membership and team leadership	