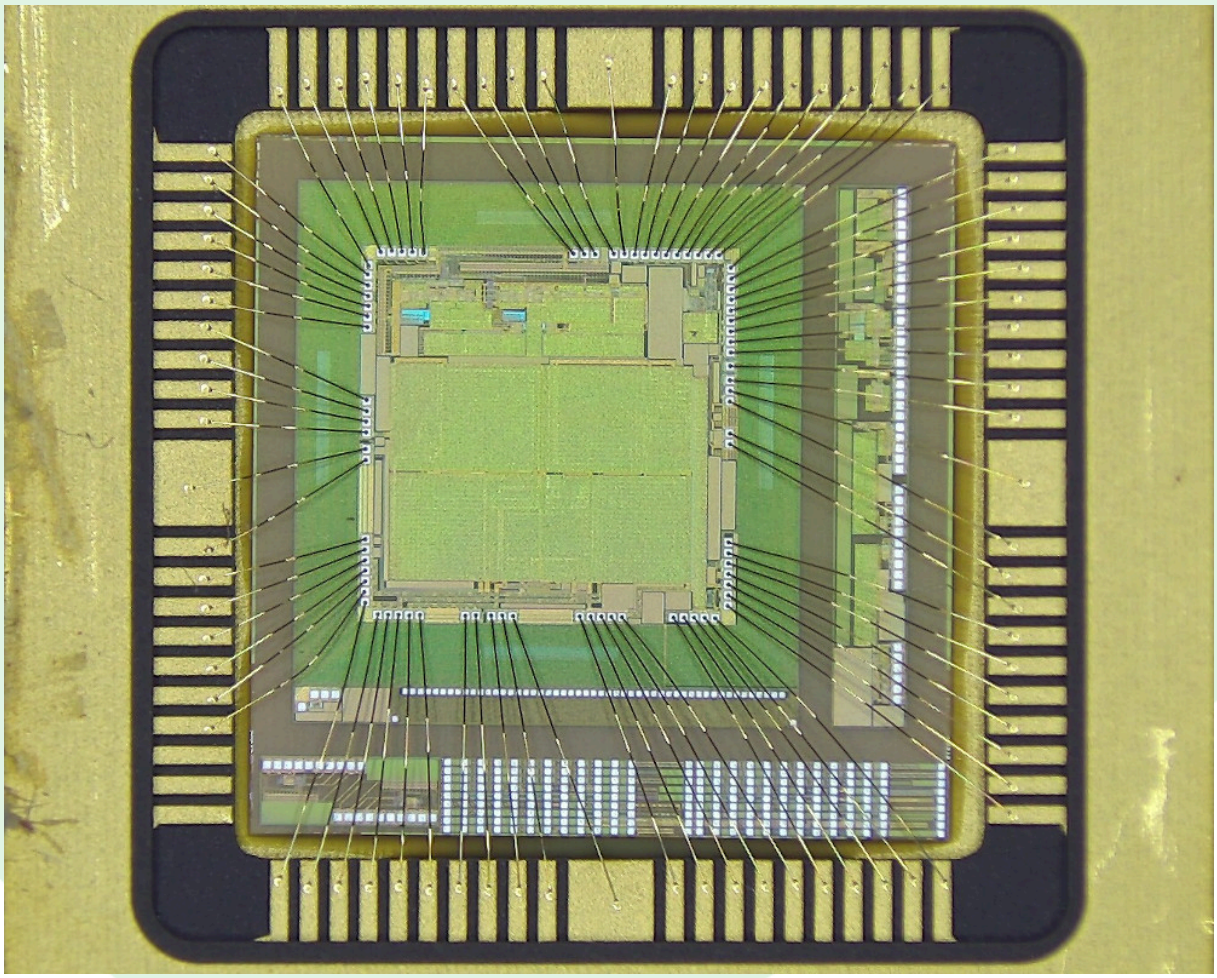
ELEC9701

Mixed Signal Microelectronic Design

Term 3, 2022



Course Overview

Staff Contact Details

Convenors

Name	Email	Availability	Location	Phone
Torsten Lehmann	t.lehmann@unsw.edu.au	Tuesdays 12-1pm, Thursdays 4-5pm	G17-343	93855374

School Contact Information

Consultations: Lecturer consultation times will be advised during the first lecture. You are welcome to email the tutor or laboratory demonstrator, who can answer your questions on this course and can also provide you with consultation times. ALL email enquiries should be made from your student email address with ELEC/TELExxxx in the subject line; otherwise they will not be answered.

Keeping Informed: Announcements may be made during classes, via email (to your student email address) and/or via online learning and teaching platforms – in this course, we will use Moodle https://moodle.telt.unsw.edu.au/login/index.php. Please note that you will be deemed to have received this information, so you should take careful note of all announcements.

Student Support Enquiries

For enrolment and progression enquiries please contact Student Services

Web

Electrical Engineering Homepage

Engineering Student Support Services

Engineering Industrial Training

UNSW Study Abroad and Exchange (for inbound students)

UNSW Future Students

Phone

(+61 2) 9385 8500 – Nucleus Student Hub

(+61 2) 9385 7661 – Engineering Industrial Training

(+61 2) 9385 3179 – UNSW Study Abroad and UNSW Exchange (for inbound students)

Email

Engineering Student Support Services – current student enquiries

- e.g. enrolment, progression, clash requests, course issues or program-related queries

Engineering Industrial Training – Industrial training questions

UNSW Study Abroad – study abroad student enquiries (for inbound students)

UNSW Exchange – student exchange enquiries (for inbound students)

UNSW Future Students – potential student enquiries

- e.g. admissions, fees, programs, credit transfer

Course Details

Units of Credit 6

Summary of the Course

Special IC processes, high-voltage, silicon-on-insulator, nano scale CMOS. Scaling, process variation, matching, layout for matching. Parasitics and wire models. Advanced transistor modelling, velocity saturation, sub-threshold. High-frequency analysis. Cascode OTAs, fully-differential circuits, rail-to-rail circuits, power outputs, biasing and references. Trimming. Active filters, switched capacitor circuits, transconductors and Gm-C filters. Non-linear circuits. Schmitt triggers and charge pumps. Sigma-delta converters and automatic calibration. Logic effort. Advanced logic families, rationed logic, special functions, PLLs. Dynamic logic, TSP registers, timing, clock distribution, self-timed systems. Packaging, latch-up, I/O design, ESD, shielding and mixed analogue-digital design. Current research.

Course Aims

Background

Microelectronics or integrated electronics are the miniaturised electronic circuits that make up Integrated Circuits (ICs) such as microprocessors, Field-Programmable Gate Arrays, Flash-memories, operational amplifier, analogue-to-digital converters and many other functions. Most ICs today are implemented in various flavours of CMOS technology which is the focus of this course. The ability to use large number of components at relative low cost and the ability to match components accurately on-chip makes the design of integrated circuits and systems different from a similar design using discrete components. Mixed Signal Microelectronics Design is a broad based, more advanced IC design course, which present the students with analogue and digital circuits and design techniques required to implement mixed-signal integrated circuits with good performance.

Aims

The course aims to enable the student to do analysis and design of integrated circuits of good performance, and to equip the student to do self-guided, continuing learning in the advancing field of microelectronics.

Course Learning Outcomes

After successfully completing this course, you should be able to:

Learning Outcome	EA Stage 1 Competencies
1. Appreciate capabilities and limitations of advanced microelectronic (or IC) technologies	PE1.3, PE1.4
2. Understand and use advanced circuit models of IC components	PE1.2, PE1.3
3. Analyse analogue and digital microelectronic circuits	PE1.1, PE1.2, PE1.3, PE1.5, PE2.1, PE2.2, PE2.3
4. Design analogue, digital and mixed microelectronic circuits	PE1.3, PE1.5, PE2.1, PE2.2,

Learning Outcome	EA Stage 1 Competencies
	PE2.3, PE3.2, PE3.3, PE3.4, PE3.5
5. Critically read and present papers from technical journals	PE1.3, PE1.4, PE2.2, PE3.2, PE3.3, PE3.4, PE3.5
6. Keep up-to-date with future technological development in the field	PE1.3, PE1.4, PE2.2

Targeted Graduate Capabilities

Electrical Engineering and Telecommunications programs are designed to address the following targeted capabilities which were developed by the school in conjunction with the requirements of professional and industry bodies:

- The ability to apply knowledge of basic science and fundamental technologies;
- The skills to communicate effectively, not only with engineers but also with the wider community;
- The capability to undertake challenging analysis and design problems and find optimal solutions;
- Expertise in decomposing a problem into its constituent parts, and in defining the scope of each part;
- A working knowledge of how to locate required information and use information resources to their maximum advantage;
- Proficiency in developing and implementing project plans, investigating alternative solutions, and critically evaluating differing strategies;
- An understanding of the social, cultural and global responsibilities of the professional engineer;
- The ability to work effectively as an individual or in a team;
- An understanding of professional and ethical responsibilities;
- The ability to engage in lifelong independent and reflective learning.

UNSW Graduate Capabilities

The course delivery methods and course content directly or indirectly addresses a number of core UNSW graduate capabilities, as follows:

- Developing scholars who have a deep understanding of their discipline, through discussion classes and design task.
- Developing rigorous analysis, critique, and reflection, and ability to apply knowledge and skills to solving problems, through tutorial exercises and design task.
- Developing capable independent and collaborative enquiry, through discussion classes.
- Developing digital and information literacy and lifelong learning skills, through lectures, class preparations and report writing.
- Developing the capability of effective communication, through report writing.
- Developing independent, self-directed professionals who are enterprising, innovative, creative and responsive to change, through the design task.

Teaching Strategies

Delivery Mode

- Formal lectures, which provide you with a focus on the core analytical material in the course,

together with qualitative, alternative explanations and individually targeted illustrations to aid your understanding.
- Self-guided tutorials, which allow for exercises in problem solving and allow time for you to resolve in-depth problems for quantitative understanding of the lecture material.
- Discussion classes, which practice critical analysis and detailed discussion of design engineer's primary source of knowledge for keeping abreast a rapidly developing field: research papers.
- A design task, which draws together theoretical and practical design aspects in an open-ended realistic design problem, reinforcing the course material.

Learning in this Course

You are expected to attend all lectures, discussion classes, and quizzes, in order to maximise your learning. You must prepare well for discussion classes and your participation will be assessed. You should read relevant sections of the recommended texts. Lecture notes will not be given: reading and reflecting on the recommended texts and identify critical parts with the aid of the lectures is an essential component of this course. Reading additional texts will further enhance your learning experience. Group learning is also encouraged. UNSW assumes that self-directed study of this kind is undertaken in addition to attending face-to-face classes throughout the course.

Lectures

During the lectures technology capabilities and design issues are discussed and theoretical aspects of IC design and technology are presented. Numerous examples of analogue and digital integrated circuit functions are discussed in order to convey a qualitative understanding of circuit operations. You are encouraged to actively engage in the lectures to facilitate two-way communication and enhance learning. The lectures aim to support you in analysing and designing integrated circuits, and to help you appreciate the capabilities of IC technologies.

Self-guided Tutorials

You should attempt all of the problem sheet questions provided. Group learning is encouraged. Answers to these questions may be discussed during the consultation time.

Discussion Classes

Technical papers are the researcher's and practicing design engineer's primary source of knowledge for keeping abreast a rapidly developing field. During the discussion classes, and on-line prior to classes, students and lecturer will discuss papers from technical journals; from week 2 onwards, students will take turns to lead these discussions. The discussion classes thus provide you with exercises in critically analysing and reflective learning from technical papers; they also provide you with exercise in oral communication and with advanced, contemporary discipline knowledge. The discussion classes aim to prepare you for future self-guided learning. You are required to participate in the discussion classes.

Design Task

The design task aims to draw together theoretical and practical design aspects in an open-ended realistic design problem. You will design an integrated circuit meeting given specifications, use the CAD tools to verify the circuit operation and write a report in the form of a technical paper documenting your design. The design task provide and test engineering creativity, open-ended problem solving skills, communication skills and general understanding of the course content. You may use the CAD tools in room G17-202/G17-217 for this task.

Additional Course Information

Relationship to Other Courses

This is a graduate level course in the School of Electrical Engineering and Telecommunications. It is offered to students following a post-graduate program at the university and is a requirement for students doing research in the area of integrated circuit design.

Pre-requisites and Assumed Knowledge

The course builds on the integrated circuit design foundations given in the undergraduate course ELEC4602, Microelectronics Design and Technology. ELEC4602 is a pre-requisite for this course, but the two courses can be followed concurrently. It is essential that you have good working knowledge of circuit theory, basic analogue and digital electronics, and basic signal analysis as covered in the courses ELEC1112, Electrical Circuits, ELEC2133, Analogue Electronics, ELEC2141, Digital Circuit Design, ELEC2134, Circuits and Signals, and ELEC3106, Electronics which is the pre-requisite course for ELEC4602. It is finally assumed that you are proficient in the use of personal computers and are familiar with SPICE-type circuit simulation.

Assessment

The assessment scheme in this course reflects the intention to assess your learning progress through the term. Ongoing assessment occurs through the discussion classes, and class-time quizzes.

Assessment task	Weight	Due Date	Course Learning Outcomes Assessed
1. Design Task	15%	Not Applicable	3, 4
2. Discussion classes	15%	Not Applicable	1, 5, 6
3. Quizzes	10%	Not Applicable	1, 2, 3
4. Final Examination	60%	Not Applicable	2, 3, 4, 6

Assessment 1: Design Task

Submission notes: See Moodle for laboratory report submission dates.
Deadline for absolute fail: Five days after the design report submission deadline.

The design task is assessed to test your ability to design an integrated circuit and communicate its key features in a professional manner, thus also demonstrating your appreciation of the technology, your ability to use appropriate models and simulations, and your ability to conduct suitable analysis to aid in the design.

You should maintain a lab book and must record suitable screen shots or print-outs as documentation for your work. The design and verification work must be documented in a report which is due Monday the due week listed in the course schedule. The report must take the form of a four-page technical paper (IEEE format). Late submissions carry a 5% penalty per day and will not be accepted beyond five days delay. Delays on medical grounds are accepted. Each report must be uploaded as a .pdf file (no other format accepted) on the course Moodle site.

Assessment criteria

Assessment marks (grade only) will be awarded on the basis of your report according to your understanding of the design problem, simulations carried out, the quality and innovativeness of your design, and your ability to concisely explain and characterise your design in your report. A HD mark is given only for exceptional performance that exceed design requirements; a serious attempt at completing the problem is required for a PS mark.

Assessment 2: Discussion classes

Participation and engagement in the discussion classes are assessed in order to ensure that the students are able to critically read and learn from technical papers, and communicate their findings to the class. Students must post discussion items (questions, answers, observations, etc) related to each weeks discussion paper on Moodle prior to each discussion class.

Assessment criteria

Assessment is grade-only marks and are given on basis on activeness of participation and on the ability

to learn from the papers and to lead the discussions. A HD mark is given only for exceptional performance and engagement; active participation is required for a PS mark.

Assessment 3: Quizzes

Submission notes: See Moode for quiz dates and times.

There are two quizzes held during the lecture time through the term. These are designed to give early feedback on your progress through the theoretical components of the course and test your general understanding of the course material. Questions will be drawn from course material covered in the four weeks prior to each quiz.

Assessment criteria

Assessment marks are given according the correct fraction of the answers to the quiz questions.

Assessment 4: Final Examination

The exam in this course is an open-book 2 hour written examination. University approved calculators are allowed. The examination tests analytical and critical thinking and general understanding of the course material in a controlled fashion. Questions may be drawn from any aspect of the course (including discussion classes), unless specifically indicated otherwise by the lecturer.

Assessment criteria

Assessment marks will be assigned according to the correctness of the responses.

Hurdle requirement

An examination mark of at least 45% is required to pass the course.

Attendance Requirements

Students are strongly encouraged to attend all classes and review lecture recordings.

Course Schedule

View class timetable

Timetable

Date	Type	Content
Week 1: 12 September - 16 September	Lecture	Advanced CMOS technologies and components.
	Reading	Notes.
	Topic	Self-directed: technology scaling. JB ch. 6, Notes.
	Seminar	Discussion topic 0: integrated technology/devices.
Week 2: 19 September - 23 September	Lecture	Process variations, parasitics, wire models, non-linear capacitances.
	Reading	JB ch. 3, 4, 5, Notes.
	Topic	Self-directed: layout matching. JB ch. 5, 20.
	Seminar	Discussion topic 1: integrated technology/devices.
Week 3: 26 September - 30 September	Lecture	Advanced MOS models and matching models.
	Reading	JB ch. 9, 10, Notes.
	Seminar	Discussion topic 2: integrated technology/devices.
Week 4: 3 October - 7 October	Lecture	Advanced cascodes and HF analysis.
	Reading	JB ch. 20, 21, 22.
	Seminar	Discussion topic 3: integrated analogue circuits.
	Assessment	**Quiz 1**.
Week 5: 10 October - 14 October	Lecture	Advanced operational amplifier design.
	Reading	JB ch. 24, 26, 23.
	Seminar	Discussion topic 4: integrated analogue circuits.
Week 6: 17 October - 21 October	Lecture	Active filters and non-linear circuits.
	Reading	JB ch. 25, 27, Notes.
	Seminar	Discussion topic 5: integrated analogue circuits.
Week 7: 24 October -	Lecture	Advanced A/D converter design.

28 October	Reading	JB ch. 29, Notes.
	Seminar	Discussion topic 6: integrated analogue circuits.
Week 8: 31 October - 4 November	Lecture	Advanced logic, sizing, special functions, PLLs.
	Reading	JB ch. 11, 12, 18, 19, Notes.
	Topic	Self-directed: logic effort. Notes.
	Seminar	Discussion topic 7: integrated digital circuits.
	Assessment	**Quiz 2**.
Week 9: 7 November - 11 November	Lecture	Dynamic logic, registers and timing.
	Reading	JB ch. 13, 14, Notes.
	Seminar	Discussion topic 8: integrated digital circuits.
Week 10: 14 November - 18 November	Lecture	Packaging, I/O and mixed-signal design.
	Reading	JB ch. 1, 3, 4, Notes.
	Seminar	Discussion topic 9: integrated digital circuits.
Study Week: 21 November - 24 November	Assessment	**Project Report** due.

Resources

Prescribed Resources

Textbook

- R. J. Baker, CMOS Circuit Design, Layout, and Simulation. Wiley Interscience, 3rd/4th ed., 2010/2019.

On-line resources

Moodle: As a part of the teaching component, Moodle will be used to upload project reports and host forums, including a discussion classes forum. Moodle will also be used to disseminate discussion papers. Assessment marks will also be made available via Moodle: https://moodle.telt.unsw.edu.au/login/index.php.
Course webpage: The course webpage is used to disseminate course material, including design brief, past assessment and examination papers, and some lecture notes: https://subjects.ee.unsw.edu.au/elec9701.
Teams: Teams (accessed using your University zpass credentials) will be used for any required on-line real-time communications and lecture recordings: https://teams.microsoft.com/.

CAD resources

Students can access the industry standard Cadence design suite for the work in this course. The CAD tools are located in the computer laboratories G17-202 and G17-217. Students must remember to copy their work on to their own storage device before they logout as all data will otherwise be lost. For specific details on how to log on, see the course web page. Students who have not followed ELEC4602 are encouraged to go through the ELEC4602 laboratory exercises in order to familiarise themselves with the CAD tools.

Remote computer access

Computers in rooms G17-202 and G17-217 can be accessed remotely via https://aaa-access.unsw.edu.au/vpn/index.html. Click on DESKTOPS and subsequenty ELECENG-LABPC-G17-Rm202 or ELECENG-LABPC-G17-Rm217 to start a Citrix remote session on a computer in one of those rooms. Students must have the Citrix Workspace player (download from https://www.citrix.com/en-au/downloads/workspace-app/) installed on their own computer.

Recommended Resources

Reference books

- T. C. Carusone, D. A. Johns and K. W. Martin, Analog Integrated Circuit Design. Wiley and Sons Inc., 2nd ed., 2012.
- T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits. Cambridge University Press, 1998.
- N. Weste and D. Harris, CMOS VLSI Design: a Circuits and Systems Perspective. Addison-Wesley, 3rd ed., 2005.

Course Evaluation and Development

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the Course and Teaching Evaluation and Improvement Process. You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings. As a result of previous feedback obtained for this course, and in our efforts to provide a rich and meaningful learning experience, we have changed the weighting of in-term assessments, increased the number of tutorial exercises, released summary slides, and commenced the use of on-line discussion tools.

Academic Honesty and Plagiarism

Academic Honesty and Plagiarism

Plagiarism is the unacknowledged use of other people's work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a form of academic misconduct, and the University has very strict rules that include some severe penalties. For UNSW policies, penalties and information to help you avoid plagiarism, see https://student.unsw.edu.au/plagiarism. To find out if you understand plagiarism correctly, try this short quiz: https://student.unsw.edu.au/plagiarism-quiz.

General Conduct and Behaviour

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and students may be asked to leave the class.

Academic Information

COVID19 - Important Health Related Notice

Your health and the health of those in your class is critically important. You must stay at home if you are sick or have been advised to self-isolate by NSW health or government authorities. Current alerts and a list of hotspots can be found here. **You will not be penalised for missing a face-to-face activity due to illness or a requirement to self-isolate**. We will work with you to ensure continuity of learning during your isolation and have plans in place for you to catch up on any content or learning activities you may miss. Where this might not be possible, an application for fee remission may be discussed.

If you are required to self-isolate and/or need emotional or financial support, please contact the Nucleus: Student Hub. If you are unable to complete an assessment, or attend a class with an attendance or participation requirement, please let your teacher know and apply for special consideration through the Special Consideration portal. To advise the University of a positive COVID-19 test result or if you suspect you have COVID-19 and are being tested, please fill in this form.

UNSW requires all staff and students to follow NSW Health advice. Any failure to act in accordance with that advice may amount to a breach of the Student Code of Conduct. Please refer to the Safe Return to Campus guide for students for more information on safe practices.

Dates to note

Important Dates available at: https://student.unsw.edu.au/dates

Student Responsibilities and Conduct

Students are expected to be familiar with and adhere to all UNSW policies (see https://student.unsw.edu.au/policy), and particular attention is drawn to the following:

Workload

It is expected that you will spend at least **15 hours per week** studying a 6 UoC course, from Week 1 until the final assessment, including both formal classes and *independent, self-directed study*. In periods where you need to complete assignments or prepare for examinations, the workload may be greater. Over-commitment has been a common source of failure for many students. You should take the required workload into account when planning how to balance study with employment and other activities.

Attendance

Regular and punctual attendance at all classes is expected. UNSW regulations state that if students attend less than 80% of scheduled classes they may be refused final assessment.

Work Health and Safety

UNSW policy requires each person to work safely and responsibly, in order to avoid personal injury and to protect the safety of others.

Special Consideration and Supplementary Examinations

You must submit all assignments and attend all examinations scheduled for your course. You can apply for special consideration when illness or other circumstances beyond your control interfere with an assessment performance. If you need to submit an application for special consideration for an exam or assessment, you must submit the application **prior to the start** of the exam or before the assessment is submitted, except where illness or misadventure prevent you from doing so. Be aware of the "fit to sit/submit" rule which means that if you sit an exam or submit an assignment, you are declaring yourself well enough to do so and cannot later apply for Special Consideration. For more information and how to apply, see https://student.unsw.edu.au/special-consideration.

Administrative Matters

On issues and procedures regarding such matters as special needs, equity and diversity, occupational health and safety, enrolment, rights, and general expectations of students, please refer to the School and UNSW policies:

https://student.unsw.edu.au/guide

https://www.engineering.unsw.edu.au/electrical-engineering/resources

Disclaimer

This Course Outline sets out description of classes at the date the Course Outline is published. The nature of classes may change during the Term after the Course Outline is published. Moodle should be consulted for the up-to-date class descriptions. If there is any inconsistency in the description of activities between the University timetable and the Course Outline (as updated in Moodle), the description in the Course Outline/Moodle applies.

Image Credit

Chip wirebonded in package (c) 2019 Torsten Lehmann

CRICOS

CRICOS Provider Code: 00098G

Acknowledgement of Country

We acknowledge the Bedegal people who are the traditional custodians of the lands on which UNSW Kensington campus is located.

Appendix: Engineers Australia (EA) Professional Engineer Competency Standard

Program Intended Learning Outcomes	
Knowledge and skill base	
PE1.1 Comprehensive, theory based understanding of the underpinning natural and physical sciences and the engineering fundamentals applicable to the engineering discipline	✓
PE1.2 Conceptual understanding of the mathematics, numerical analysis, statistics, and computer and information sciences which underpin the engineering discipline	✓
PE1.3 In-depth understanding of specialist bodies of knowledge within the engineering discipline	✓
PE1.4 Discernment of knowledge development and research directions within the engineering discipline	✓
PE1.5 Knowledge of engineering design practice and contextual factors impacting the engineering discipline	✓
PE1.6 Understanding of the scope, principles, norms, accountabilities and bounds of sustainable engineering practice in the specific discipline	
Engineering application ability	
PE2.1 Application of established engineering methods to complex engineering problem solving	✓
PE2.2 Fluent application of engineering techniques, tools and resources	✓
PE2.3 Application of systematic engineering synthesis and design processes	✓
PE2.4 Application of systematic approaches to the conduct and management of engineering projects	
Professional and personal attributes	
PE3.1 Ethical conduct and professional accountability	
PE3.2 Effective oral and written communication in professional and lay domains	✓
PE3.3 Creative, innovative and pro-active demeanour	✓
PE3.4 Professional use and management of information	✓
PE3.5 Orderly management of self, and professional conduct	✓
PE3.6 Effective team membership and team leadership	