Course Outline

Term 2, 2021

DESN2000-ELEC Engineering Design and Professional Practice

Units of Credit	**6**
Contact hours	6 per week

DESN2000 will give students skills for creating innovative design concepts in the context of a embedded systems engineering project. The course aims to further develop your skills in engineering design with a particular focus on the early stages, where innovative concepts are created in response to open-ended problems.

This course uses both Moodle and Microsoft Teams as the portal for remote teaching and learning. It will be used for file sharing, virtual classrooms, announcements and other communications. You are expected to check the platforms regularly. In the first instance, you are encouraged to ask questions after lectures and during labs. Otherwise course discussions and questions take place on the Moodle discussion forum. Your demonstrators and academic staff will actively monitor these posts. Please use replies and keep discussions in appropriate channels. If required, emails must be made from your student email address with DESN2000 in the subject line.

Your class times may vary week to week. Please check your myUNSW timetable for your class times each week.

Faculty Coordinators	Prof Ilpo Koskinen
	Dr Doménique van Gennip
	Dr Nicholas Gilmore
	Design Next, Kens J17 Lv5 Rm503 (designnext@unsw.edu.au)
School Coordinator and Lecturer	David Tsai (d.tsai@unsw.edu.au)
	Bioscience South Kens E26, Lv1 Rm1003
Demonstrators	TBD

INFORMATION ABOUT THE COURSE

Prerequisites and assumed knowledge

The pre-requisites for this course comprise ENGG1000 (Engineering Design & Innovation), ELEC2141 (Digital Circuit Design) and COMP1511 (Programming Fundamentals) or COMP1521 (Computer Systems Fundamentals). Students should have a good understanding, in particular, on number systems, C programming and basic computer architecture. The course shares substantial content with ELEC2142 (Embedded Systems Design), which is no longer offered. You cannot take this course after completing ELEC2142.

Following courses

This course is a pre-requisite for several EE&T courses, e.g. TELE3118 (Network technologies) and ELEC4601 (Advanced Digital and Embedded Systems Design).

Relationship to other EE&T courses

This is a 2nd year course at the School of Electrical Engineering and Telecommunications. It is a core subject for students following a BE (Electrical) or (Telecommunications) program.

COVID19 - Important Health Related Notice

Your health and the health of those in your class is critically important. You must stay at home if you are sick or have been advised to self-isolate by NSW health or government authorities. Current alerts and a list of hotspots can be found here. **You will not be penalised for missing a face-to-face activity due to illness or a requirement to self-isolate**. We will work with you to ensure continuity of learning during your isolation and have plans in place for you to catch up on any content or learning activities you may miss. Where this might not be possible, an application for fee remission may be discussed.

If you are required to self-isolate and/or need emotional or financial support, please contact the Nucleus: Student Hub. If you are unable to complete an assessment, or attend a class with an attendance or participation requirement, please let your teacher know and apply for special consideration through the Special Consideration portal. To advise the University of a positive COVID-19 test result or if you suspect you have COVID-19 and are being tested, please fill in this form.

UNSW requires all staff and students to follow NSW Health advice. Any failure to act in accordance with that advice may amount to a breach of the Student Code of Conduct. Please refer to the Safe Return to Campus guide for students for more information on safe practices.

HANDBOOK DESCRIPTION

See link to virtual handbook*:*

https://preview.handbook.unsw.edu.au/undergraduate/courses/2021/DESN2000/

OBJECTIVES

This course will give students skills for creating innovative design concepts in the context of an embedded systems engineering project. Specifically, DESN2000 aims to further develop your skills in engineering design with a particular focus on the early stages, where innovative concepts are

created in response to open-ended problems. These skills will be developed in the context of an engineering project, with a focus on three areas:

(1) research techniques needed to understand design problems and discover concepts,

(2) technical skills needed to build a concept, and

(3) evaluation methods for evaluating the concept.

Alongside the development of design skills, the course also aims to develop your readiness for professional practice by deepening your understanding and skills in effective project management, teamwork and communication.

This course combines generic design content with discipline-specific content. The common section focuses on mapping contextual information including human factors; analysis of the information; creative methods for translating the information into design concepts; communication of the information; and evaluation methods for analysing the validity of the design proposals.

Technical skills focus on the design for embedded systems. These systems are pervasive in all areas of society from sensor taps to satellites and knowledge of how to design them is a vital skill for all electrical and computer science engineers. The discipline-specific objective of this course is to equip students with the knowledge and skills that enable them to design basic embedded systems, where a microcontroller is the central element.

The first half of the course will focus on ARM processor architecture, instruction sets, assembly language fundamentals and techniques. The second half of the course will look at input and output, interrupts, and exceptions. On completion students should be able to design reliable embedded system using ARM processors in particular, and other processors in general. The course touches upon several technical topics you need in designing embedded systems:

- Binary numbers, hexadecimal numbers, signed / unsigned numbers, 2s complement, status flags and ASCII;
- Programmer's model of ARM7TDMI processor core, registers, fetch-decode-execute cycle and ARM v4T instruction set architecture (ISA);
- Assembly language programming, data processing instructions, arithmetic operations and logical operations;
- Memory access instructions, load-store architecture, word and byte addressing, memory alignment and block data transfer;
- Control flow, conditional branches, loops and jump tables;
- Functions and subroutines calls, link register, stack, stack frames, register conventions and AAPCS standard;
- Fixed-point numbers, range and precision;
- Compiler, assembler, linker, loader, assembler directives, pseudo-instructions, and object files;
- Input/output, memory mapped I/O, polling and interrupts;
- Exceptions and modes of operation.

TEACHING STRATEGIES

Delivery mode

This course will use the following teaching modes:

- Lectures, which provide you with a focus on the core analytical material of the course, together with qualitative, alternative explanations to aid your understanding;

- Laboratory sessions, which support the formal lecture material and also provide you with practical construction, measurement and debugging skills;
- Design workshops, which allow for exercises in problem solving and allow time for you to resolve problems in understanding of lecture and project material.

Students will complete both individual and group work. For each hour of contact it is expected that you will put in at least 1.5 hours of private study. It is expected that groups meet outside of the scheduled times and progress their group project independently.

All class materials for 2021 T2 will be delivered online via Moodle and some communications via MS Teams. This includes the project brief, lecture notes, lab guides, workshop guides and assessment guides. You will be added to the DESN2000 ELEC Teams instance automatically.

MS Teams and/or Blackboard Collaborate Ultra may be used for lecture recordings and virtual classrooms. Links are posted well in advance of scheduled times.

Lectures

You are expected to attend all lectures, which are all delivered online. These provide the backbone for your practical work in the workshops and your project. To help you putting the lecture knowledge into practice, there will be a short weekly Moodle exercise that you should complete by the **Sunday evening 11:59 PM**. These are **not graded, but you must complete at least 7/8 weekly exercises** to pass this course. We will provide answers to these exercises the following week.

Workshops

Weekly workshops are the primary means through which students work through their project and associated exercises aimed at developing understanding of the course materials. Demonstrators are available to provide guidance and support teams in their project development. Guides for these classes will be made available in Moodle and MS Teams.

The face-to-face workshops will be held on the allocated classes on campus. The online workshops for remote students will be delivered remotely via MS Teams and/or Blackboard Collaborate Ultra (access via Moodle). You will find links to the online sessions on MS Teams in your class channel.

Laboratories

The laboratory schedule is designed to provide practical, hands-on exposure to the concepts conveyed in lectures soon after they are covered in class. There will be 6 laboratory tasks. Each week, a new design problem related to the lectured material is presented. You will be required to step through the problem to a complete solution using the guidelines given per lab exercise. You are strongly encouraged to **read over all the material and attempt any code writing before coming to your lab session,** as it will allow you to complete the required tasks within the allocated time slot.

Throughout the labs, a NXP LPC2478 microcontroller (based on an ARM7TDMI-S core) and Keil µVision4 Integrated Development Environment (IDE) will be used.

- In the first three exercises, tasks will be focused on various fundamental assembly programming techniques: data processing, control flow, and functions.
- The interaction of the processor with inputs and outputs peripherals and handling interrupts will be the subject of the remaining labs.

Laboratory attendance WILL be kept, and **you MUST attend at least 7/8 of the labs**. There is no laboratory exemption for this course regardless of whether equivalent labs have been completed in previous courses. If, for medical reasons (a valid medical certificate must be provided), you are unable to attend a lab, you will need to apply for a catch-up lab during another lab time, as agreed by the laboratory coordinator.

All local students will attend on-campus labs, unless agreed otherwise with course authority. For remote students, the labs will be accessible remotely, through strategies that have been standardized across many large-cohort EE&T courses. A MS Teams setup will be configured for you and your lab partner to control the lab PC remotely and to communicate with your demonstrator. A live feed of the LPC2478 board, plus an internet-enabled oscilloscope, provide real-time access. Your demonstrator (and generally, also an assistant demonstrator) will be physically present in the lab to help with any issue.

EXPECTED LEARNING OUTCOMES

This course is designed to address the learning outcomes above and the corresponding Engineers Australia Stage 1 Competency Standards for Professional Engineers as shown. The full list of Stage 1 Competency Standards may be found in Appendix C.

Learning outcomes		
#	**Learning outcome description**	**EA stage 1 Competencies**
1	Develop design concepts using standard methods to collect, assess and intergrate end user, stakeholder and project requirements.	1.5, 2.1, 2.2, 2.3, 3.3
2	Validate the suitability of designs using standard technical methods, while considering end-user and stakeholder contexts.	1.5, 1.6, 2.1, 2.2, 2.3, 3.3
3	Implement disciplinary technical theory and skills pertinent to the design project. Specific displinary learning outcomes: • 3.1 Demonstrate an understanding of what an embedded system is, and what its main components are. • 3.2 Demonstrate competency in working with and manipulating fixed-point number systems. • 3.3 Demonstrate understanding of assembly language programming fundamentals. • 3.4 Demonstrate the principles of “good” embedded software design. • 3.5 Demonstrate an understanding of 32-bit ARM processor architecture. • 3.6 Demonstrate an understanding of mapping high-level instructions to low-level elementary instructions. • 3.7 Use a mix of C and assembly to design embedded systems containing interrupts, multitasking, and I/O.	1.3, 2.1, 2.2, 2.3 1.1, 1.2 1.2 1.1, 1.2 1.3, 1.5, 3.1 1.3, 2.1 1.3 1.3, 2.2
4	Contribute to the work of a team and collaborate on the design project, including the implementation of organisational and interpersonal tools.	2.4, 3.3, 3.4, 3.5, 3.6
5	Integrate project management techniques to plan, execute and complete an open-ended design project.	2.4, 3.4
6	Explain designs to various audiences using oral, written, and visual forms of professional and persuasive communication.	3.2

^ This course is designed to provide the above learning outcomes, which arise from targeted, graduate capabilities listed in ***Appendix A***. The targeted graduate capabilities broadly support the UNSW and Faculty of Engineering graduate capabilities (listed in ***Appendix B***). This course also addresses the Engineers Australia (National Accreditation Body) Stage I competency standard as outlined in ***Appendix C***.

COURSE PROGRAM

Class Topics

Date	Lectures	Lab (ElecENG 119) *	Workshop *
Week 1 31/05/2021	David Tsai Tue 14-17. 3 hour. Introduction to ARM. Ilpo Koskinen Wed 13-14. 1 hour. Course introduction and the basic of concept design.	*(no lab this week)*	Demonstrator Various times. 2 hours Introduction to project and pressure cooker exercise.
Week 2 07/06/2021	David Tsai Tue 14-17. 3 hour. Data processing operations and memory access. Simon Gorta Wed 12-13. 1 hour. Guest lecture from a conservation ecologist specialising in birds. Ilpo Koskinen Wed 13-14. 1 hour. User research for concept design.	*(no lab this week)*	Demonstrator Various times. 2 hours Guided workshop on developing a user research plan to support concept design.
Week 3 14/06/2021	David Tsai Tue 14-17. 3 hour. Control flow and conditional operations. Nick Gilmore Wed 13-14. 1 hour. User research analysis and ideation.	Demonstrator Various times. 3 hours 1. Introduction to QVGA board, µVision, and debugging.	Demonstrator Various times. 2 hours Guided workshop on user research analysis.
Week 4 21/06/2021	David Tsai Tue 14-17. 3 hour. Functions, subroutines, and AAPCS.	Demonstrator Various times. 3 hours 2.1 Data types, control flow, assembly programming	Demonstrator Various times. 2 hours Guided workshop on concept ideation.
Week 5 28/06/2021	David Tsai Tue 14-17. 3 hour. AAPCS and I/O interface (Introduction to GPIO).	Demonstrator Various times. 3 hours 2.2 Data types, control flow, assembly programming	Demonstrator Various times. 2 hours Guided workshop on defining your unique value proposition.
Week 6** 05/07/2021	David Tsai Tue 14-17. 3 hour. Revision of earlier material.	Demonstrator Various times. 3 hours 3. Functions and subroutines	Demonstrator Various times. 2 hours Optional revision/consultation session.

Date	Lectures	Lab (ElecENG 119) *	Workshop *
Week 7 12/07/2021	David Tsai Tue 14-17. 3 hour. I/O interface (GPIO, UART, DAC). Doménique van Gennip Wed 13-14. 1 hour. User testing and the design process.	Demonstrator Various times. 3 hours 4. I/O	Demonstrator Various times. 2 hours Workshop topic TBD.
Week 8 19/07/2021	David Tsai Tue 14-17. 3 hour. Pseudo instructions and literal pools. Shahe Momdjian Wed 13-14. 1 hour. Pitching techniques and convincing engineering presentations.	Demonstrator Various times. 3 hours 5.1 D/A conversion	Demonstrator Various times. 2 hours Guided workshop on pitching.
Week 9 26/07/2021	David Tsai Tue 14-17. 3 hour. Exceptions & interrupts.	Demonstrator Various times. 3 hours 5.2 D/A conversion	Demonstrator Various times. 2 hours Guided time with demonstrators to work on your pitch video, or otherwise work on the project.
Week 10** 02/08/2021	David Tsai Tue 14-17. 3 hour. Revision of earlier material.	Demonstrator Various times. 3 hours 6. LCD & touchscreen	Demonstrator Various times. 2 hours Free time to work on final project deliverables with demonstrator support.

** Please check your myUNSW timetable for specific lab and workshop times.*

*** No new content or assignment submission during week 6 due to flexibility week.*

Class Schedule

Please check your myUNSW timetable for your individual timetable information, and for any announcements on Moodle and Microsoft Teams.

Week 1	Week 2	Week 3	Week 4	Week 5	Revision	Week 7	Week 8	Week 9	Week 10
Lecture *Introduction to ARM* Tue 14-17	**Lecture** *Data processing operations and memory access* Tue 14-17	**Lecture** *Control flow and conditional operations* Tue 14-17	**Lecture** *Functions, subroutines, and AAPCS* Tue 14-17	**Lecture** *AAPCS and I/O interface (Introduction, GPIO)* Tue 14-17	**Lecture** *Revision* Tue 14-17	**Lecture** *I/O interface (GPIO, UART, DAC)* Tue 14-17	**Lecture** *Pseudo instructions and literal pools* Tue 14-17	**Lecture** *Exceptions & interrupts* Tue 14-17	**Lecture** *Revision* Tue 14-17
Lecture *Concept design* Wed 13-14	**Lecture** *Research in design* Wed 13-14	**Lecture** *User research analysis* Wed 13-14				**Lecture** *User testing* Wed 13-14	**Lecture** *Pitching* Wed 13-14		
	Guest lecture *Simon Gorta* Wed 12-13	**Lab** *1. Introduction to QVGA board, µVision and debugging* ElecENG 119	**Lab** *2.1 Data types, control flow, assembly programming* ElecENG 119	**Lab** *2.2 Data types, control flow, assembly programming* ElecENG 119	**Lab** *3. Functions and subroutines* ElecENG 119	**Lab** *4. I/O* ElecENG 119	**Lab** *5.1 D/A conversion* ElecENG 119	**Lab** *5.2 D/A conversion* ElecENG 119	**Lab** *6. LCD & touchscreen* ElecENG 119
Workshop *Project pressure cooker*	**Workshop** *User research plan*	**Workshop** *User research data analysis*	**Workshop** *Ideation*	**Workshop** *Unique Value Proposition*	**Workshop** *Revision*	**Workshop** *(TBD)*	**Workshop** *Guided pitching*	**Workshop** *Pitch practice*	**Workshop** *Revision*
			Journal *12.5 %*					**Journal** *12.5%*	**Design prezi** *15%*
		Labs 8x *(20 %)*							

ASSESSMENTS

Assessment Outline

Item	Weighting	Learning outcomes	Assessment criteria	Due date by
Design Journal (👤)				
End of week 4	12.5 %	1-6	Refer to assessment guide	11:59 PM, Friday 25 June (Week 4)
End of week 9	12.5 %	1-6	Refer to assessment guide	11:59 PM, Sunday 01 August (Week 9)
Weekly lab exercises (👥)	20 %	3	Refer to assessment guide	Weekly as per lab schedule (Weeks 3-10)
Design presentation (👥)	15 %	1-6	Refer to assessment guide	11:59 PM, Sunday 08 August (Week 10)
Final exam (👤)	40 %	1-6	Refer to assessment guide	Exam period, TBD

(👤) individual assessment. (👥) group assessment.

Details for each assessment are presented in separate assessment guides for each task.

Individual contribution to the Design presentation will be evaluated via a team evaluation survey for each submission.

Marks will be returned within 2 weeks of the submission due date.

PENALTIES

Late work will be penalised at the rate of 10% per day after the due time and date have expired.

Completion of 7/8 labs and 7/8 weekly exercises are compulsory for successful completion of DESN2000. Exception (e.g. due to medical reasons) from these requirements will need approval from Nucleus Student Hub and/or course authority.

RELEVANT RESOURCES

- van Roeijen, Annemiek et al. 2015. Delft Design Guide. BIS Publisher, Amsterdam. Second edition.
- William Hohl, ARM Assembly Language: Fundamentals and Techniques, CRC Press, 2015 (2nd Edition).
- Steve Furber, ARM System On-Chip, 2nd Edition, Addison-Wesley, 2000.

Online resources:

Moodle and Microsoft Teams will be used to disseminate teaching materials. Assessment marks will also be made available via Moodle: https://moodle.telt.unsw.edu.au/login/index.php.

Refer to Academic Advice on the School website, for information about:

- Notes on assessments and plagiarism
- School policy on Supplementary exams
- Special Considerations
- Solutions to Problems,
- Year Managers and Grievance Officer of Teaching and Learning Committee, and

DATES TO NOTE

Refer to MyUNSW for Important Dates available at: https://student.unsw.edu.au/dates

PLAGIARISM

Beware! An assignment that includes plagiarised material will receive a 0% Fail, and students who plagiarise may fail the course. Students who plagiarise are also liable to disciplinary action, including exclusion from enrolment.

Plagiarism is the unacknowledged use of other people's work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a form of academic misconduct, and the University has very strict rules that include some severe penalties. For UNSW policies, penalties and information to help you avoid plagiarism see https://student.unsw.edu.au/plagiarism. To find out if you understand plagiarism correctly, try this short quiz: https://student.unsw.edu.au/plagiarism-quiz.

WORKLOAD

It is expected that you will spend at least **15 hours per** week studying a 6 UoC course, from Week 1 until the final assessment, including both face-to-face classes and independent, self-directed study. In periods where you need to complete assignments or prepare for examinations, the workload may be greater. Over-commitment has been a common source of failure for many

students. You should take the required workload into account when planning how to balance study with employment and other activities.

Regular and punctual attendance at all classes is expected. UNSW regulations state that if students attend less than 80% of scheduled classes they may be refused final assessment.

GENERAL CONDUCT & BEHAVIOUR

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and students may be asked to leave the class.

WORK HEALTH & SAFETY

UNSW policy requires each person to work safely and responsibly, in order to avoid personal injury and to protect the safety of others.

SPECIAL CONSIDERATION & SUPPLEMENTARY EXAMINATION

You must submit all assignments and attend all examinations scheduled for your course. You can apply for special consideration when illness or other circumstances beyond your control interfere with an assessment performance. If you need to submit an application for special consideration for an exam or assessment, you must submit the application **prior to the start** of the exam or before the assessment is submitted, except where illness or misadventure prevent you from doing so. Be aware of the "fit to sit/submit" rule which means that if you sit an exam or submit an assignment, you are declaring yourself well enough to do so and cannot later apply for Special Consideration. For more information and how to apply, see https://student.unsw.edu.au/special-consideration.

COURSE IMPROVEMENT

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the online student survey myExperience.

You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings. As a result of previous feedback obtained for this course and in our efforts to provide a rich and meaningful learning experience, we have continued to evaluate and modify our delivery and assessment methods including updated lecture notes, workshops, blended learning resources, in-class demonstrations, and industry guest lectures.

ADMINISTRATIVE MATTERS

All students are expected to read and be familiar with UNSW guidelines and polices. In particular, students should be familiar with the following:

- Special Considerations: student.unsw.edu.au/special-consideration;
- Exams: https://student.unsw.edu.au/exams
- Approved Calculators: https://student.unsw.edu.au/exam-approved-calculators-and-computers
- Academic Honesty and Plagiarism: https://student.unsw.edu.au/plagiarism
- Equitable Learning Services: https://student.unsw.edu.au/els
- General and Program-specific questions: The Nucleus: Student Hub

- Others: https://student.unsw.edu.au/support

Appendix A: Targeted Graduate Capabilities

Electrical Engineering and Telecommunications programs are designed to address the following targeted capabilities which were developed by the school in conjunction with the requirements of professional and industry bodies:

- The ability to apply knowledge of basic science and fundamental technologies;
- The skills to communicate effectively, not only with engineers but also with the wider community;
- The capability to undertake challenging analysis and design problems and find optimal solutions;
- Expertise in decomposing a problem into its constituent parts, and in defining the scope of each part;
- A working knowledge of how to locate required information and use information resources to their maximum advantage;
- Proficiency in developing and implementing project plans, investigating alternative solutions, and critically evaluating differing strategies;
- An understanding of the social, cultural and global responsibilities of the professional engineer;
- The ability to work effectively as an individual or in a team;
- An understanding of professional and ethical responsibilities;
- The ability to engage in lifelong independent and reflective learning.

Appendix B: UNSW Graduate Capabilities

The course delivery methods and course content directly or indirectly addresses a number of core UNSW graduate capabilities, as follows:

- Developing scholars who have a deep understanding of their discipline, through lectures and solution of analytical problems in tutorials and assessed by assignments and written examinations.
- Developing rigorous analysis, critique, and reflection, and ability to apply knowledge and skills to solving problems. These will be achieved by the laboratory experiments and interactive checkpoint assessments and lab exams during the labs.
- Developing capable independent and collaborative enquiry, through a series of tutorials spanning the duration of the course.
- Developing digital and information literacy and lifelong learning skills through assignment work.

Appendix C: Engineers Australia (EA) Competencies

Stage 1 Competencies for Professional Engineers

	Program Intended Learning Outcomes
PE1: Knowledge and Skill Base	PE1.1 Comprehensive, theory-based understanding of underpinning fundamentals
	PE1.2 Conceptual understanding of underpinning maths, analysis, statistics, computing
	PE1.3 In-depth understanding of specialist bodies of Knowledge
	PE1.4 Discernment of knowledge development and research directions
	PE1.5 knowledge of engineering design practice
	PE1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice
PE2: Engineering Application Ability	PE2.1 Application of established engineering methods to complex problem solving
	PE2.2 Fluent application of engineering techniques, tools and resources
	PE2.3 Application of systematic engineering synthesis and design processes
	PE2.4 Application of systematic approaches to the conduct and management of engineering projects
PE3: Professional and Personal Attributes	PE3.1 Ethical conduct and professional accountability
	PE3.2 Effective oral and written communication (professional and lay domains)
	PE3.3 Creative, innovative and pro-active demeanour
	PE3.4 Professional use and management of information
	PE3.5 Orderly management of self, and professional conduct
	PE3.6 Effective team membership and team leadership