School of Electrical Engineering and Telecommunications

Term 1, 2021
Course Outline

ELEC2141
Digital Circuit Design

COURSE STAFF

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Consultations: Lecturer consultation times will be advised during the first lecture. You are welcome to email the tutor or laboratory demonstrator, who can answer your questions on this course and can also provide you with consultation times. ALL email enquiries should be made from your student email address with ELEC2141 in the subject line; otherwise they will not be answered.

Keeping Informed: Announcements may be made during classes, via email (to your student email address) and/or via online learning and teaching platforms – in this course, we will use Moodle https://moodle.telt.unsw.edu.au/login/index.php. Please note that you will be deemed to have received this information, so you should take careful note of all announcements.

COURSE SUMMARY

Contact Hours

The course consists of pre-recorded videos lectures available online, two 1-hour discussion sessions, a 1-hour tutorial, and a 2-hour laboratory session each week. Both tutorials and labs will begin in Week 2.

	Day	Time	Location
Lectures	**Pre-recorded videos available on Moodle**		
Discussions	Monday	4 - 5pm	Microsoft Teams Meeting
	Thursday	4 - 5pm	Microsoft Teams Meeting
Tutorials			
T12A	Tuesday	12pm – 1pm	Quad G034
T13A	Tuesday	1pm – 2pm	TETB G16
T14A	Tuesday	2pm – 3 pm	Quad 1043
W10A	Wednesday	10am – 11am	TETB G16
W12A	Wednesday	12pm – 1pm	Biosci G07
W13A	Wednesday	1pm – 2pm	Microsoft Teams Meeting
H12A	Thursday	12pm – 1pm	Ainswth101
F12A	Friday	12pm – 1pm	TETB G16
F13A	Friday	1pm – 2pm	Quad G034
Labs			
M09A	Monday	9am – 11am	EE119
M13A	Monday	1pm – 3pm	EE119
T09A	Tuesday	9am – 11am	EE119
T11A	Tuesday	11am – 1 pm	EE119
T14A	Tuesday	2 pm – 4 pm	EE119
T16A	Tuesday	4 pm – 6 pm	EE119
W09A	Wednesday	9am – 11am	EE119
W11A	Wednesday	11am – 1 pm	EE119

W14A	Wednesday	2 pm – 4 pm	EE119
W16A	Wednesday	4 pm – 6 pm	EE119
H09A	Thursday	9am – 11am	EE119
H11A	Thursday	11am – 1 pm	EE119
H13A	Thursday	1pm – 3pm	EE119
F09A	Friday	9am – 11am	EE119
F11A	Friday	11am – 1 pm	EE119
F14A	Friday	2 pm – 4 pm	EE119
F16A	Friday	4 pm – 6 pm	Microsoft Teams Meeting

Context and Aims

Digital circuits are integral parts of many areas of engineering and technology such as personal computers, digital signal processing, telecommunications, speech analysis and recognition, and control systems. The objective of this course is to equip students with the necessary fundamental knowledge and skill that enable them to understand, analyze and design digital circuits in the real world. The first half of the course will focus on the analysis and design of combinational and sequential logic circuits. VHSIC Hardware Description Language, arithmetic circuits (VHDL), computer design fundamentals and CMOS and TTL technologies will be covered in the second half of the course. At the completion of the course, students should be in a position to be able to design and build reliable and cost effective digital circuits. The course aims to provide students with fundamental knowledge of digital systems with respect to several different levels of abstraction – from a low-level dealing with electrical circuits through to a high-level dealing with software tools and hardware description languages.

Indicative Lecture Schedule

Period	Summary of Lecture Program
Week 1	Introduction to digital systems, number systems & combinational logic circuits
Week 2	Combinational logic circuit analysis
Week 3	Combinational logic circuit design
Week 4	Sequential circuit elements and analysis
Week 5	Sequential circuit design/**Mid-term exam (March 18, 4-5 pm)**
Week 6	Flexibility Week/Revision
Week 7	Verilog HDL/**Assignment 1 due (March 29, 6pm)**
Week 8	Arithmetic circuits
Week 9	Computer design fundamentals
Week 10	Digital logic families and CMOS technology/**Assignment 2 due (April 19, 6pm)**

Indicative Laboratory Schedule

Period	Summary of Laboratory Program
Week 1	No labs
Week 2	Introduction to digital circuits,
Week 3	Xilinx ISE, Digilent Nexys 3 & FPGA programming
Week 4	Combinational circuit design
Week 5	Flip-Flop basics
Week 6	No labs/Catch up labs (Optional)
Week 7	Sequential circuit design
Week 8	Counters and 7-segment display
Week 9	Electronic handball game design
Week 10	Lab exam

Assessment

Laboratory experiments (weekly lab session + final lab exam)	20%
Assignments (I & II)	20%
Midterm assessments (exam + fortnightly quizzes)	20%
Final Exam	40%

COVID19 - Important Health Related Notice

Your health and the health of those in your class is critically important. You must stay at home if you are sick or have been advised to self-isolate by NSW health or government authorities. Current alerts and a list of hotspots can be found here. **You will not be penalised for missing a face-to-face activity due to illness or a**

requirement to self-isolate. We will work with you to ensure continuity of learning during your isolation and have plans in place for you to catch up on any content or learning activities you may miss. Where this might not be possible, an application for fee remission may be discussed.

If you are required to self-isolate and/or need emotional or financial support, please contact the Nucleus: Student Hub. If you are unable to complete an assessment, or attend a class with an attendance or participation requirement, please let your teacher know and apply for special consideration through the Special Consideration portal. To advise the University of a positive COVID-19 test result or if you suspect you have COVID-19 and are being tested, please fill in this form.

UNSW requires all staff and students to follow NSW Health advice. Any failure to act in accordance with that advice may amount to a breach of the Student Code of Conduct. Please refer to the Safe Return to Campus guide for students for more information on safe practices.

COURSE DETAILS

Credits

This is a 6 UoC course and the expected workload is 15 hours per week throughout the 10-week term.

Relationship to Other Courses

This is a 2nd year course in the School of Electrical Engineering and Telecommunications. It is a core course for students following a BE (Electrical) or (Telecommunications) program.

Pre-requisites and Assumed Knowledge

The co-requisite for this course is ELEC1111: Electrical Circuit Fundamentals, which introduced basic concepts of electrical circuits. It is further assumed that you have a good computer literacy.

Following Courses

The course is a pre-requisite for DESN2000: Engineering Design and Professional Practice, in which the digital system design concepts introduced in ELEC2141 will be applied extensively. It is also a pre-requisite for ELEC3106: Electronics in which low level analysis and implementation of various logic gates are undertaken.

Learning outcomes

After successful completion of this course, you should be able to:

1. Analyze and design combinational circuits
2. Explain the workings of standard digital circuit elements e.g. multiplexers, decoders, etc. and use them to design simple digital circuits
3. Design and optimize simple synchronous sequential circuits
4. Describe the fundamental components in the central processing unit (CPU) of a computer and the operations these components perform.
5. Develop digital circuits to solve practical, real world problems and describe their use in more complex systems.
6. Construct various hardware implementations using basic digital circuit elements and explain how they operate.
7. Demonstrate basic skills in working with computer-aided design tools, including knowing the rudiments of a hardware description language (VHDL).
8. Implement simple designs using a range of components, from basic digital circuit elements to programmable logic devices.

This course is designed to provide the above learning outcomes which arise from targeted graduate capabilities listed in ***Appendix A***. The targeted graduate capabilities broadly support the UNSW and Faculty of Engineering graduate capabilities (listed in ***Appendix B***). This course also addresses the Engineers Australia (National Accreditation Body) Stage I Competency Standards as outlined in ***Appendix C***.

Syllabus

Introduction to digital systems, number systems, binary numbers, base conversion, binary codes. Binary variables, logical operators, logic gates, Boolean functions, Boolean algebra, standard forms, two-level optimization, Karnaugh maps, don't-care conditions, multi-level optimization, high-impedance outputs. Combinational logic design procedures, technology mapping, function blocks, multi-bit variables, encoders, decoders, multiplexers, demultiplexers. Sequential circuits, basic storage elements, latches and flip-flops structures, direct inputs, finite state machines, transition equations, state tables and diagrams, state assignments, logic diagrams, Mealy and Moore models, state minimization. Arithmetic circuits, half and full adders, cascading adders, signed numbers and 2's complements, subtractors. Programmable devices, FPGAs, hardware description languages, Verilog implementations, simulations. Introduction to computer design, datapaths, arithmetic/logic unit (ALU), shifters, instructions set. Integrated circuits (ICs), CMOS technology, CMOS logic gates.

TEACHING STRATEGIES

Delivery Mode

The teaching in this course aims at establishing a good fundamental understanding of the areas covered using:

- Online pre-recorded video lectures, which provide you with a focus on the core analytical material in the course, together with qualitative, alternative explanations to aid your understanding;
- Discussion sessions, which you provide you with the opportunity to engage with the lecturer, discuss material presented in the recorded lectures and ask questions to clarify any doubts;
- Tutorials, which allow for exercises in problem solving and allow time for you to resolve problems in understanding of lecture material;
- Laboratory sessions, which support the formal lecture material and also provide you with practical construction, measurement and debugging skills;

Learning in this course

You are expected to attend all lectures, tutorials, labs, and mid-term exams in order to maximise learning. You must prepare well for your laboratory classes and your lab work will be assessed. In addition to the lecture notes/video, you should read relevant sections of the recommended text. Reading additional texts will further enhance your learning experience. Group learning is also encouraged. UNSW *assumes* that self-directed study of this kind is undertaken in addition to attending formal classes throughout the course.

Pre-recording video lecture recordings

The lectures form the core of this subject. Topics presented in lectures will generally be followed by detailed examples to provide students with the real-life applications. Detailed explanations of the topics will be available to students in the form of lecture notes and the prescribed textbook.

Discussion sessions

Discussion sessions will be held in the scheduled lecture times where the key material and examples presented in the lecture videos will be revised and students provided the opportunity to ask questions about concepts that need clarification.

Tutorial classes

Tutorial classes will be held in Weeks 2-10. You should attempt all of your problem sheet questions in advance of attending the tutorial classes. The importance of adequate preparation prior to each tutorial cannot be overemphasized, as the effectiveness and usefulness of the tutorial depends to a large extent on this preparation. Group learning is encouraged. Answers for these questions will be discussed during the tutorial class and the tutor will cover the more complex questions in the tutorial class. In addition, during the tutorial class, 1-2 new questions that are not in your notes may be provided by the tutor, for you to try in class. These questions and solutions may not be made available on the web, so it is worthwhile for you to attend your tutorial classes to gain maximum benefit from this course.

Laboratory program

The laboratory schedule is deliberately designed to provide practical, hands-on exposure to the concepts conveyed in lectures. Each week a new design problem is presented. Students will be required to step through the problem to a complete solution using the guidelines given as per lab exercise. The laboratory exercises cover a wide scope ranging from using breadboards and discrete IC components to using industry-standard design software and FPGA implementation. The exercise will follow similar (although simplified) design procedures used in industry. Students will need to bring their own breadboards previously used in ELEC1111 to the laboratory. Breadboards will also be offered for sale through the school office.

A broad understanding of the tools utilized in these exercises is highly encouraged and a bonus lab task will be available to students after the successful completion of all other exercises. The bonus task will carry on from the last lab exercise and will be accompanied by minimal guidelines, allowing students to further demonstrate their ability to analyse and resolve issues independently. There are two optional labs which students are encourage to carry out for an extra lab mark on the top of the bonus task. These optional labs should be done under minimal supervision and only considered or marked after the student has finished all mandatory labs.

You are required to attend laboratory from week 2 to week 10. Laboratory attendance WILL be kept, and you MUST attend at least 80% of the labs. Prior to attending each lab, you must read over each lab in the lab manual and complete the pre-lab quiz on Moodle before each session. You will not be allowed to start the lab unless you have answered all the questions in the pre-lab quiz.

The laboratory manual will be uploaded on Moodle. Every student should have the hard-bound copy of the laboratory manual and must bring it to the laboratory class. Marks will be recorded on the laboratory manual. In addition to the laboratory manual, you should also bring a lab pack. The lab pack should be collected from G1 (EE&T) prior to attending your first laboratory class. The lab pack will contain all hardware components you will need for the entire lab. Without the hardware components in the lab pack, you will not be able to do some of the laboratory activities and therefore it is important you bring you lab pack to the laboratory class. The first lab pack will be given for free. After the first one, you will be expected to pay.

The laboratory schedule is deliberately designed to provide practical exposure to the concepts conveyed in lectures soon after they are covered in class. You are required to attend laboratory. Laboratory attendance WILL be kept, and you MUST attend at least 80% of labs.

More details of the online laboratory plan for the online laboratory session will be announced through Moodle announcements in Week 1.

Laboratory Exemption

There is no laboratory exemption for this course. Regardless of whether equivalent labs have been completed in previous courses, all students enrolled in this course must take the labs. If, for medical reasons, (note that a valid medical certificate must be provided) you are unable to attend a lab, you will need to apply for a catch-up lab during another lab time, as agreed by the laboratory coordinator.

ASSESSMENT

The assessment scheme in this course reflects the intention to assess your learning progress through the term. Ongoing assessment occurs through the lab checkpoints (see lab manual), lab exam, mid-term assessments and two assignments.

Laboratory Experiments

The laboratory experiments will be assessed in two parts: weekly laboratory assessments worth 15% in total and a final lab exam in week 10 worth 5%.

1. **Laboratory Assessment**

   Laboratories are primarily about learning, and the laboratory assessment is designed mainly to check your knowledge as you progress through each stage of the laboratory tasks. It is essential that you complete the laboratory preparation before coming to the lab. **This includes reading over each lab in the lab manual and completing the pre-lab quiz on Moodle before each session. Students will not be allowed to start the lab unless they have answered all the questions in the pre-lab quiz. Students will have unlimited attempts to complete the pre-lab quiz.** Each lab exercise will have one check point that will be marked by the laboratory demonstrators. Although there is only one check point for each lab, there are several results that students are required to demonstrate when marked for the check point. Therefore, you are strongly advised to (i) record results on the lab manual; (ii) save the accomplished tasks or results on working directory in the lab PC; (iii) keep the working circuit on the breadboard for the laboratory demonstrators to check. Laboratory demonstrators will be available to help students with any questions or difficulties.

   Upon completion of a checkpoint, students will be required to write down their student and bench numbers on the Laboratory Queue Sheet and wait for the laboratory assessor to mark their work. Students may continue working on subsequent lab tasks while waiting to be assessed. Students will be required to show the working of their task for each checkpoint and answer questions asked by the laboratory assessor to demonstrate their understanding of the ideas addressed within each task.

Students will work in pairs but be marked individually. Each student will be asked a few questions. There will also be a mark for the group based on demonstrating the required lab tasks. Refer to the laboratory manual for the marking guideline.

Assessment marks will be awarded according to your preparation (completing set preparation exercises and correctness of these or readiness for the lab in terms of pre-reading), how much of the lab you were able to complete, your understanding of the experiments conducted during the lab, the quality of the code you write during your lab work (according to the guidelines given in lectures), and your understanding of the topic covered by the lab.

After completing each experiment, your work will be assessed by the laboratory demonstrator. Both the results sheet and your lab book will be assessed by the laboratory demonstrator.

Assessment marks will be awarded according to your preparation (completing set preparation exercises and correctness of these or readiness for the lab in terms of pre-reading), how much of the lab you were able to complete, your understanding of the experiments conducted during the lab, the quality of the code you write during your lab work (according to the guidelines given in lectures), and your understanding of the topic covered by the lab.

2. **Laboratory Exam**

   To check that you have achieved the practical learning outcomes for the course, you will be examined in the laboratory. Laboratory Exams are closed book practical exams that will assess your technical understanding of using design software tools used throughout the labs in simulating, verifying, and implementing digital circuits on the FPGA board. You will be given two design problems, asked to implement and verify the design on the FPGA board. Marks will be awarded for the correct understanding of practical and relevant theoretical concepts, correct operation of laboratory equipment, and correct interpretation of measured results.

Mid-Term Assessment

The midterm assessment has two parts: fortnightly quizzes worth 5% and an open book online mid-term exam in week 5 worth 15%.

1. **Fortnight online quizzes -** There will be fortnightly quizzes throughout the semester. The purpose of the quizzes is to keep students up-to-date with the lecture material and to test basic understanding of the course concepts. The fortnightly quizzes will make up 5% of the overall mark. Each quiz will consist of a number of randomly selected multiple choice questions from a pool of questions so that students may not have exactly the same set of questions. The quiz will be marked according to the number of correct answers. The quizzes are a mandatory component of the overall assessment and failure to attempt a quiz will result in no marks being given for the quiz. Each quiz will be available for a period of two weeks and the results per quiz will be published at the end of the period. No late attempts will be permitted. **Students must attempt all 4 fortnightly quizzes to pass this subject. Quizzes should be attempted genuinely and independently. If Moodle suspects dependent and insincere practices, it will alert the course convener.**

   The quizzes are delivered through Moodle and will each be made available for a period of two weeks between every Saturday at 9:00am (week 1, 3, 5, 7) to the following Saturday at 11:59pm (weeks 3, 5, 7, 9) after which a new quiz will become available.

2. **Mid-Term Exam**

   The midterm exam in this course is a standard closed-book 1-hour written examination, comprising two compulsory questions. It accounts for 15% of the overall mark. University approved calculators are allowed. The examination tests analytical and critical thinking and general understanding of the course material in a controlled fashion. Questions will be drawn from the topics covered in the first four weeks of the course, unless specifically indicated otherwise by the lecturer. Marks will be assigned according to the correctness of the responses. The exam will be held will be held on March 18, 2021 from 4pm to 5pm (During the first hour of week 5 Thursday lecture).

Assignments

The assignments, which will consist of design challenges, form 20% of the overall mark. There will be two assignments for this subject due at the end of week 6 and 9. The assignments will be released at the end of week

2 and week 6, respectively, on Moodle. The assignments will consist of one or more design problems and students are required to provide a complete design solution with verified implementations. All relevant workings, schematic diagrams, HDL codes, and simulations results must be attached to the submissions. All submissions must be made electronically via Moodle. **Assignment 1 is due on March 29, 6pm (Monday, Week 7). Assignment 2 is due on April 19, 6pm (Monday, Week 10). No late submission will be possible after the due time.**

Though generic guidelines will be provided, there will be no one "correct" solution to the assignments. Students will be expected to work independently on their implementation and to be able to justify the unique design choices along the way.

Final Exam

The exam in this course is a two-hour written examination, comprising three compulsory questions. It accounts for 40% of the overall mark. University approved calculators are allowed. The examination tests analytical and critical thinking and general understanding of the course material in a controlled fashion. Questions may be drawn from any aspect of the course (including laboratory), unless specifically indicated otherwise by the lecturer. Marks will be assigned according to the correctness of the responses.

Relationship of Assessment Methods to Learning Outcomes

	Learning outcomes							
Assessment	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Laboratory practical assessments	✓	✓	✓	-	-	✓	✓	✓
Lab exam	✓	✓	-	-	-	-	✓	✓
Fortnight online quizzes	✓	✓	✓	✓	-	✓	✓	-
Assignment	✓	✓	✓	-	✓	-	✓	✓
Midterm exam	✓	✓	-	-	-	✓	-	-
Final exam	-	-	✓	✓	✓	✓	✓	-

COURSE RESOURCES

Textbooks

Prescribed textbook

- M. Mano, C. R. Kime and T. Martin, Logic and Computer Design Fundamentals, 5th Edition (Global Edition), Pearson, 2016.
- M. Mano, C. R. Kime, Logic and Computer Design Fundamentals, 4th Edition, Prentice Hall, 2008

Reference books

- R. H. Katz & G. Borriello, Contemporary Logic Design, 2nd Edition, Prentice Hall, 2005,
- M. Mano & M. D. Cilietti, Digital Design, 4th Edition, Prentice Hall, 2007.
- J. F. Wakerly, Digital Design: Principles and Practices, 4th Edition, Prentice Hall, 2006

On-line resources

Moodle

As a part of the teaching component, Moodle will be used to disseminate teaching materials, host forums and occasionally, quizzes. Assessment marks will also be made available via Moodle: https://moodle.telt.unsw.edu.au/login/index.php.

Mailing list

Announcements concerning course information will be given in the lectures and/or on Moodle and/or via email (which will be sent to your student email address).

OTHER MATTERS

Dates to note

Important Dates available at: https://student.unsw.edu.au/dates

Academic Honesty and Plagiarism

Plagiarism is the unacknowledged use of other people's work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a form of academic misconduct, and the University has very strict rules that include some severe penalties. For UNSW policies, penalties and information to help you avoid plagiarism, see https://student.unsw.edu.au/plagiarism. To find out if you understand plagiarism correctly, try this short quiz: https://student.unsw.edu.au/plagiarism-quiz.

Student Responsibilities and Conduct

Students are expected to be familiar with and adhere to all UNSW policies (see https://student.unsw.edu.au/policy), and particular attention is drawn to the following:

Workload

It is expected that you will spend at least **15 hours per week** studying a 6 UoC course, from Week 1 until the final assessment, including both formal classes and *independent, self-directed study*. In periods where you need to complete assignments or prepare for examinations, the workload may be greater. Over-commitment has been a common source of failure for many students. You should take the required workload into account when planning how to balance study with employment and other activities.

Attendance

Regular and punctual attendance at all classes is expected. UNSW regulations state that if students attend less than 80% of scheduled classes they may be refused final assessment.

General Conduct and Behaviour

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and students may be asked to leave the class.

Work Health and Safety

UNSW policy requires each person to work safely and responsibly, in order to avoid personal injury and to protect the safety of others.

Special Consideration and Supplementary Examinations

You must submit all assignments and attend all examinations scheduled for your course. You can apply for special consideration when illness or other circumstances beyond your control interfere with an assessment performance. If you need to submit an application for special consideration for an exam or assessment, you must submit the application **prior to the start** of the exam or before the assessment is submitted, except where illness or misadventure prevent you from doing so. Be aware of the "fit to sit/submit" rule which means that if you sit an exam or submit an assignment, you are declaring yourself well enough to do so and cannot later apply for Special Consideration. For more information and how to apply, see https://student.unsw.edu.au/special-consideration.

Continual Course Improvement

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the online student survey myExperience. You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings. As a result of previous feedback obtained for this course and in our efforts to provide a rich and meaningful learning experience, we have continued to evaluate and modify our delivery and assessment methods.
More time will be spent in the lectures on Verilog and CMOS technology. The students use the online lecture recordings extensively so more details recordings will be created to better support their learning. Additional problem solving videos will be created and provided to the students.

Administrative Matters

On issues and procedures regarding such matters as special needs, equity and diversity, occupational health and safety, enrolment, rights, and general expectations of students, please refer to the School and UNSW policies:
https://student.unsw.edu.au/guide
https://www.engineering.unsw.edu.au/electrical-engineering/resources

APPENDICES

Appendix A: Targeted Graduate Capabilities

Electrical Engineering and Telecommunications programs are designed to address the following targeted capabilities which were developed by the school in conjunction with the requirements of professional and industry bodies:

- The ability to apply knowledge of basic science and fundamental technologies;
- The skills to communicate effectively, not only with engineers but also with the wider community;
- The capability to undertake challenging analysis and design problems and find optimal solutions;
- Expertise in decomposing a problem into its constituent parts, and in defining the scope of each part;
- A working knowledge of how to locate required information and use information resources to their maximum advantage;
- Proficiency in developing and implementing project plans, investigating alternative solutions, and critically evaluating differing strategies;
- An understanding of the social, cultural and global responsibilities of the professional engineer;
- The ability to work effectively as an individual or in a team;
- An understanding of professional and ethical responsibilities;
- The ability to engage in lifelong independent and reflective learning.

Appendix B: UNSW Graduate Capabilities

The course delivery methods and course content directly or indirectly addresses a number of core UNSW graduate capabilities, as follows:

- Developing digital and information literacy and lifelong learning skills through assignment work.
- Developing ethical practitioners who are collaborative and effective team workers, through group activities, seminars and tutorials.
- Developing independent, self-directed professionals who are enterprising, innovative, creative and responsive to change, through challenging design and project tasks.
- Developing citizens who can apply their discipline in other contexts, are culturally aware and environmentally responsible, through interdisciplinary tasks, seminars and group activities.

Appendix C: Engineers Australia (EA) Professional Engineer Stage 1 Competency Standards

Competency Standards		Learning Outcomes
PE1: Knowledge and Skill Base	PE1.1 Comprehensive, theory-based understanding of underpinning fundamentals	1-7
	PE1.2 Conceptual understanding of underpinning maths, analysis, statistics, computing	1-7
	PE1.3 In-depth understanding of specialist bodies of knowledge	1-7
	PE1.4 Discernment of knowledge development and research	

	directions	
	PE1.5 Knowledge of engineering design practice	1-7
	PE1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice	
PE2: Engineering Application Ability	PE2.1 Application of established engineering methods to complex problem solving	1-7
	PE2.2 Fluent application of engineering techniques, tools and resources	1-7
	PE2.3 Application of systematic engineering synthesis and design processes	
	PE2.4 Application of systematic approaches to the conduct and management of engineering projects	
PE3: Professional and Personal Attributes	PE3.1 Ethical conduct and professional accountability	
	PE3.2 Effective oral and written communication (professional and lay domains)	5,6
	PE3.3 Creative, innovative and pro-active demeanour	5, 6, 8
	PE3.4 Professional use and management of information	5, 6, 8
	PE3.5 Orderly management of self, and professional conduct	
	PE3.6 Effective team membership and team leadership	5, 6, 8