Course Outline

Term 2, 2020

DESN2000-EE&T Engineering Design and Professional Practice

COURSE DETAILS

Units of Credit	**6**
Contact hours	6-8 per week

DESN2000 uses Microsoft Teams as the portal for remote teaching and learning. It will be used for file sharing, virtual classrooms, announcements and other communications. You are expected to check the platform regularly. In the first instance, you are encouraged to ask questions after lectures. Otherwise course discussions and questions take place in *Posts* on MS Teams. Your demonstrators and academic staff will actively monitor these posts. Please use replies and keep discussions in appropriate channels. If required, emails must be made from your student email address with DESN2000 in the subject line.

Your class times will often vary week to week. Please check your myUNSW timetable for your class times each week.

Course Coordinator and Lecturer	Ilpo Koskinen ilpo.koskinen@unsw.edu.au Design Next, Kens J17 Lv5 Rm503
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Workshop demonstrators	Oishik Sarkar o.sarkar@unsw.edu.au Hangyue Lui hangyue.liu@unsw.edu.au

INFORMATION ABOUT THE COURSE

Prerequisites and assumed knowledge

The pre-requisites for this course comprise ENGG1000 (Engineering Design & Innovation), ELEC2141 (Digital Circuit Design) and COMP1511 (Programming Fundamentals) or COMP1521 (Computer Systems Fundamentals). Students should have a good understanding, in particular, on number systems, C programming and basic computer architecture. The course shares substantial content with ELEC2142 (Embedded Systems Design), which is no longer offered. You cannot take this course after completing ELEC2142.

Following courses

This course is a pre-requisite for several EE&T courses, e.g. TELE3118 (Network technologies) and ELEC4601 (Advanced Digital and Embedded Systems Design).

Relationship to other EE&T courses

This is a 2nd year course at the School of Electrical Engineering and Telecommunications. It is a core subject for students following a BE (Electrical) or (Telecommunications) program.

HANDBOOK DESCRIPTION

See link to virtual handbook*:*

https://www.handbook.unsw.edu.au/undergraduate/courses/2020/DESN2000

OBJECTIVES

This course develops basic conceptual design skills you need in electrical engineering. The course teaches two types of design skills. Generic design skills include models of design process, economic and practical reasoning behind concept design, research and concept creation techniques in design, evaluation techniques in design, as well as communication, project management, and teamwork techniques.

Technical design skills include skills you need to design embedded systems. These systems are pervasive in all areas of society from sensor taps to satellites and knowledge of how to design them is a vital skill for all electrical engineers. The discipline-specific objective of this course is to equip students with the knowledge and skills that enable them to design basic embedded systems, where a microcontroller is the central element. The first half of the course will focus on ARM processor architecture, instruction sets, assembly language fundamentals and techniques. The second half of the course will look at input and output, interrupts, and exceptions. On completion students should be able to design reliable embedded system using ARM processors in particular and other processors in general. The course touches upon several technical topics you need in designing embedded systems:

- Binary numbers, hexadecimal numbers, signed / unsigned numbers, 2s complement, status flags and ASCII;
- Programmer's model of ARM7TDMI processor core, registers, fetch-decode-execute cycle and ARM v4T instruction set architecture (ISA);
- Assembly language programming, data processing instructions, arithmetic operations and logical operations;
- Memory access instructions, load-store architecture, word and byte addressing, memory alignment and block data transfer;
- Control flow, conditional branches, loops and jump tables;
- Functions and subroutines calls, link register, stack, stack frames, register conventions and AAPCS standard;
- Fixed-point numbers, range and precision;
- Instructions format and instructions encoding/decoding;
- Compiler, assembler, linker, loader, assembler directives, pseudo-instructions, object files and relocation tables;
- Input/output, memory mapped I/O, polling and interrupts;
- Exceptions, software interrupts, traps, modes of operation, user mode and privileged mode, vector table.

TEACHING STRATEGIES

Delivery mode

This course will use the following teaching modes:

- Lectures, which provide you with a focus on the core analytical material of the course, together with qualitative, alternative explanations to aid your understanding;
- Laboratory sessions, which support the formal lecture material and also provide you with practical construction, measurement and debugging skills;
- Design workshops, which allow for exercises in problem solving and allow time for you to resolve problems in understanding of lecture and project material.

Students will complete both individual and group work.

All class materials for 2020 T2 will be delivered online via MS Teams. This includes the project brief, lecture notes, lab guides, workshop guides and assessment guides.

Team: *DESN2000 ELEC – 2020 T2* > **Channel:** *General* > **Tab:** *Files*

MS Teams, Blackboard Collaborate Ultra and/or Zoom may be used for lecture recordings and virtual classrooms. These will all be accessed via MS Teams. Links are posted well in advance of scheduled times.

Lectures

You are expected to attend all lectures. You should also attempt all questions in the weekly exercises in advance of the Thursday afternoon lecture. We will spend the last 30 minutes of this

lecture discussing answers to these questions and to cover more complex questions. The importance of adequate preparation cannot be overemphasized, as the effectiveness and usefulness of these guided exercise sessions depends to a large extent on prior preparation. Group learning is encouraged.

Workshops

Workshops will focus on concept design and pitching. In Term 2 in 2020 the workshops will be delivered remotely via Blackboard Collaborate Ultra or Zoom, using “break-out” sessions it provides. You will find links to these sessions on your private class channel in MS Teams in due course. Workshop guides for these classes are available in MS Teams.

Laboratories

The laboratory schedule is deliberately designed to provide practical, hands-on exposure to the concepts conveyed in lectures soon after they are covered in class. There will be 7 laboratory tasks. Each week, a new design problem related to the lectured material is presented. You will be required to step through the problem to a complete solution using the guidelines given per lab exercise. You are strongly encouraged to **read over all the material and attempt any code writing before coming to your lab session,** as it will allow you to complete the required tasks within the allocated time slot.

Throughout the labs, a NXP LPC2478 microcontroller (based on an ARM7TDMI-S core) and Keil µVision4 Integrated Development Environment (IDE) will be used.

- In the first three exercises, tasks will be focused on various fundamental assembly programming techniques: data processing, control flow, and functions.
- The interaction of the processor with inputs and outputs peripherals and handling interrupts will be the subject of the remaining labs.

Laboratory attendance WILL be kept, and **you MUST attend at least 6/7 of the labs**. There is no laboratory exemption for this course regardless of whether equivalent labs have been completed in previous courses. If, for medical reasons (a valid medical certificate must be provided), you are unable to attend a lab, you will need to apply for a catch-up lab during another lab time, as agreed by the laboratory coordinator.

The labs will be accessible remotely, through strategies that have been standardized across many large-cohort EE&T T2 courses. A MS Teams setup will be configured for you and your lab partner to control the lab PC remotely and to communicate with your demonstrator. A live feed of the LPC2478 board, plus an internet-enabled oscilloscope, provide real-time access. Your demonstrator (and possibly also an assistant demonstrator) will be physically present in the lab to help with any issue.

EXPECTED LEARNING OUTCOMES

After successfully completing this course, you should be able to:

No.	Learning outcome	EA stage 1 Competencies^
1	Design creation: prepare design concepts using standard methods to collect, analyse and model user stakeholder and requirements.	1.5, 2.1, 2.3.
2	Design evaluation: verify and validate the suitability of design concepts using standard technical, economic, risk, ethical and sustainability assessments	1.5, 1.6
3	Technical knowledge: identify and acquire the technical knowledge & skills identified as necessary from the design requirements	
	3.1 Demonstrate an understanding of what an embedded system is, and what its main components are.	1.1, 1.2
	3.2 Demonstrate competency in working with and manipulating fixed-point number systems.	1.2
	3.3 Demonstrate understanding of assembly language programming fundamentals.	1.1, 1.2
	3.4 Demonstrate the principles of “good” embedded software design.	1.3, 1.5, 3.1
	3.5 Demonstrate an understanding of 32-bit ARM processor architecture.	1.3, 2.1
	3.6 Demonstrate an understanding of mapping high-level instructions to low-level elementary instructions.	1.3
	3.7 Use a mix of C and assembly to design embedded systems containing interrupts, multitasking, and I/O.	1.3, 2.2
4	Teamwork: demonstrate the characteristics of effective teamwork and professional conduct and apply organisational and interpersonal strategies	3.6
5	Project management: employ project management techniques to plan, execute and complete a design project	2.4, 3.4
6	Communication: explain designs using oral, written and visual forms of professional communication to various audiences	3.2, 3.3

^ This course is designed to provide the above learning outcomes, which arise from targeted, graduate capabilities listed in ***Appendix A***. The targeted graduate capabilities broadly support the UNSW and Faculty of Engineering graduate capabilities (listed in ***Appendix B***). This course also addresses the Engineers Australia (National Accreditation Body) Stage I competency standard as outlined in ***Appendix C***.

COURSE PROGRAM

Class Topics

Date	Lecture	Lab	Workshop
Week 1 01/06/2020	Ilpo Koskinen (1h) *Course introduction and the basics of concept design* David Tsai (2h) *Intro to embedded system, ARM and assembly language* David Tsai (2h) *Intro to embedded system, ARM and assembly language*		
Week 2 08/06/2020	David Tsai (2h) *Data processing operations and memory access* Ilpo Koskinen (1h) *Research for concept design* David Tsai (2h) *Data processing operations and memory access*		Demonstrator (1h) *Research plan*
Week 3 15/06/2020	David Tsai (2h) *Control flow and conditional operations* Ilpo Koskinen (1h) *Process for concept design* David Tsai (2h) *Control flow and conditional operations*	Demonstrator (3h) *Introduction to the QVGA base board, µVision and debugging*	Demonstrator (1h) *Ideation*
Week 4 22/06/2020	David Tsai (2h) *Functions, subroutines and procedural call standard* David Tsai (2h) *Functions, subroutines and procedural call standard*	Demonstrator (3h) *Data types and control flow*	Demonstrator (1h) *Developing concepts*

Date	Lecture	Lab	Workshop
Week 5 29/06/2020	David Tsai (2h) *Input and output interfaces* David Tsai (2h) *Input and output interfaces*	Demonstrator (3 h) *Functions and subroutines*	Demonstrator (1h) *Storytelling*
Week 6* 06/07/2020	David Tsai (2h) *Revision* David Tsai (2h) *Revision*	Demonstrator (3 h) *Inputs and outputs*	
Week 7 13/07/2020	David Tsai (2h) *Pseudo instructions, literal pools, instruction encoding & decoding* David Tsai (2h) *Pseudo instructions, literal pools, instruction encoding & decoding*	Demonstrator (3h) *Digital to analog conversion*	
Week 8 20/07/2020	David Tsai (2h) *Exceptions and interrupts* Shahe Momdijan (1h) *Guest Lecture: Pitching* David Tsai (2h) *Exceptions and interrupts*	Demonstrator (3h) *LCD and touchscreen*	Demonstrator (1h) *Pitching*
Week 9 27/07/2020	David Tsai (2h) *Revision* David Tsai (2h) *Revision & weekly exercises*	Demonstrator (3h) *Exceptions and hardware interrupts*	Demonstrator (1h) *Pitch assessment practice*
Week 10 03/08/2020		Demonstrator (3h) *Assessment – Technical presentation*	

** Flexibility week for all courses. No new content or assignment submissions.*

For each hour of contact it is expected that you will put in at least 1.5 hours of private study.

Class Schedule

Please check your myUNSW timetable for your individual timetable information, and for any announcements on Microsoft Teams.

Week 1	Week 2	Week 3	Week 4	Week 5	Week 6*	Week 7	Week 8	Week 9	Week 10
Lecture Tue. 10-12	**Lecture** Tue. 10-12	**Lecture** Tue. 10-12	**Lecture** Tue. 10-12	**Lecture** Tue. 10-12	**Lecture** Tue. 10-12	**Lecture** Tue. 10-12	**Lecture** Tue. 10-12	**Lecture** Tue. 10-12	
Lecture Mon. 17-18	**Lecture** Tue. 12-13	**Lecture** Tue. 12-13					**Lecture** Tue. 12-13		
Lecture Thur. 16-18	**Lecture** Thur. 16-18	**Lecture** Thur. 16-18	**Lecture** Thur. 16-18	**Lecture** Thur. 16-18	**Lecture** Thur. 16-18	**Lecture** Thur. 16-18	**Lecture** Thur. 16-18	**Lecture** Thur. 16-18	
		Lab Mon 12-15, Tue 13-16, Tue 16-19, Wed 12-15, Wed 15-18, Thur 9-12, Thur 12-15, Fri 12-15, Fri 15-18	**Lab** Mon 12-15, Tue 13-16, Tue 16-19, Wed 12-15, Wed 15-18, Thur 9-12, Thur 12-15, Fri 12-15, Fri 15-18	**Lab** Mon 12-15, Tue 13-16, Tue 16-19, Wed 12-15, Wed 15-18, Thur 9-12, Thur 12-15, Fri 12-15, Fri 15-18	**Lab** Mon 12-15, Tue 13-16, Tue 16-19, Wed 12-15, Wed 15-18, Thur 9-12, Thur 12-15, Fri 12-15, Fri 15-18	**Lab** Mon 12-15, Tue 13-16, Tue 16-19, Wed 12-15, Wed 15-18, Thur 9-12, Thur 12-15, Fri 12-15, Fri 15-18	**Lab** Mon 12-15, Tue 13-16, Tue 16-19, Wed 12-15, Wed 15-18, Thur 9-12, Thur 12-15, Fri 12-15, Fri 15-18	**Lab** Mon 12-15, Tue 13-16, Tue 16-19, Wed 12-15, Wed 15-18, Thur 9-12, Thur 12-15, Fri 12-15, Fri 15-18	
	Workshop Fri 12-13, Thur 14-15, Wed 11-12	**Workshop** Fri 12-13, Thur 14-15, Wed 11-12	**Workshop** Fri 12-13, Thur 14-15, Wed 11-12	**Workshop** Fri 12-13, Thur 14-15, Wed 11-12			**Workshop** Fri 12-13, Thur 14-15, Wed 11-12	**Workshop** Fri 12-13, Thur 14-15, Wed 11-12	

ASSESSMENTS

Assessment Outline

Item	Weighting	Learning outcomes	Assessment criteria	Due date
Design Journal				
Mid-term	12.5 %	1-6	See assessment guide	Midnight, Friday 3 July (Week 5)
End-term	12.5 %	1-6	See assessment guide	Midnight, Friday 7 August (Week 10)
Pitch	10 %	1-6	See assessment guide	Midnight, Friday 31 July (Week 9)
Peer Review	5 %	4-6	See assessment guide	Midnight, Friday 7 August (Week 10)
Technical Presentation	15 %	1-13	See assessment guide	Wednesday 5 – Friday 7 August (Week 10)
Laboratory				
Lab 0	2 %	3, 4, 6	See laboratory manual	End of lab
Lab 1	2 %	3, 4, 6	See laboratory manual	End of lab
Lab 2	2 %	3, 4, 6	See laboratory manual	End of lab
Lab 3	2 %	3, 4, 6	See laboratory manual	End of lab
Lab 4	2 %	3, 4, 6	See laboratory manual	End of lab
Lab 5	2 %	3, 4, 6	See laboratory manual	End of lab
Lab 6	3 %	3, 4, 6	See laboratory manual	End of lab
Final Exam	30 %	3, 4, 6		TBC

Details for each assessment are presented in separate assessment or laboratory manual for each task, except for the final exam.

Individual contribution to group assessments will be evaluated via peer review for each submission, as well as a separate peer review at the end of the term.

Marks will be returned within 2 weeks of the submission due date.

PENALTIES

Late work will be penalised at the rate of 10% per day after the due time and date have expired.

COURSE RESOURCES

- van Roeijen, Annemiek et al. 2015. *Delft Design Guide.* BIS Publisher, Amsterdam. Second edition.

Suggested readings:

- William Hohl, ARM Assembly Language: Fundamentals and Techniques, CRC Press, 2015 (2nd Edition).
- Steve Furber, ARM System On-Chip, 2nd Edition, Addison-Wesley, 2000.

Online resources:

As a part of the teaching component, Microsoft Teams and Moodle will be used to disseminate teaching materials, host forums and occasionally quizzes. Assessment marks will also be made available via Moodle: https://moodle.telt.unsw.edu.au/login/index.php.

DATES TO NOTE

Refer to MyUNSW for Important Term dates, available at: https://student.unsw.edu.au/dates

PLAGIARISM

Beware! An assignment that includes plagiarised material will receive a 0% Fail, and students who plagiarise may fail the course. Students who plagiarise are also liable to disciplinary action, including exclusion from enrolment.

Plagiarism is the unacknowledged use of other people's work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a form of academic misconduct, and the University has very strict rules that include some severe penalties. For UNSW policies, penalties and information to help you avoid plagiarism see https://student.unsw.edu.au/plagiarism. To find out if you understand plagiarism correctly, try this short quiz: https://student.unsw.edu.au/plagiarism-quiz.

WORKLOAD & ATTENDANCE

It is expected that you will spend at least **15 hours per** week studying a 6 UoC course, from Week 1 until the final assessment, including both face-to-face classes and independent, self-directed study. In periods where you need to complete assignments or prepare for examinations, the workload may be greater. Over-commitment has been a common source of failure for many students. You should take the required workload into account when planning how to balance study with employment and other activities.

Regular and punctual attendance at all classes is expected. UNSW regulations state that if students attend less than 80% of scheduled classes they may be refused final assessment.

GENERAL CONDUCT & BEHAVIOUR

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and students may be asked to leave the class.

WORK HEALTH & SAFETY

UNSW policy requires each person to work safely and responsibly, in order to avoid personal injury and to protect the safety of others.

SPECIAL CONSIDERATION & SUPPLEMENTARY EXAMINATION

You must submit all assignments and attend all examinations scheduled for your course. You can apply for special consideration when illness or other circumstances beyond your control interfere with an assessment performance. If you need to submit an application for special consideration for an exam or assessment, you must submit the application **prior to the start** of the exam or before the assessment is submitted, except where illness or misadventure prevent you from doing so. Be aware of the "fit to sit/submit" rule which means that if you sit an exam or submit an assignment, you are declaring yourself well enough to do so and cannot later apply for Special Consideration. For more information and how to apply, see https://student.unsw.edu.au/special-consideration.

COURSE IMPROVEMENT

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the online student survey myExperience. You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings. As a result of previous feedback obtained for this course and in our efforts to provide a rich and meaningful learning experience, we have continued to evaluate and modify our delivery and assessment methods including updated lecture notes, tutorials, blended learning resources, in-class demonstrations, and industry guest lectures.

ADMINISTRATIVE MATTERS

All students are expected to read and be familiar with UNSW guidelines and polices. In particular, students should be familiar with the following:

- Special Considerations: student.unsw.edu.au/special-consideration;
- Exams: https://student.unsw.edu.au/exams
- Approved Calculators: https://student.unsw.edu.au/exam-approved-calculators-and-computers
- Academic Honesty and Plagiarism: https://student.unsw.edu.au/plagiarism
- Equitable Learning Services: https://student.unsw.edu.au/els

- General and Program-specific questions: The Nucleus: Student Hub
- Others: https://student.unsw.edu.au/support

Appendix A: Targeted Graduate Capabilities

Electrical Engineering and Telecommunications programs are designed to address the following targeted capabilities which were developed by the school in conjunction with the requirements of professional and industry bodies:

- The ability to apply knowledge of basic science and fundamental technologies;
- The skills to communicate effectively, not only with engineers but also with the wider community;
- The capability to undertake challenging analysis and design problems and find optimal solutions;
- Expertise in decomposing a problem into its constituent parts, and in defining the scope of each part;
- A working knowledge of how to locate required information and use information resources to their maximum advantage;
- Proficiency in developing and implementing project plans, investigating alternative solutions, and critically evaluating differing strategies;
- An understanding of the social, cultural and global responsibilities of the professional engineer;
- The ability to work effectively as an individual or in a team;
- An understanding of professional and ethical responsibilities;
- The ability to engage in lifelong independent and reflective learning.

Appendix B: UNSW Graduate Capabilities

The course delivery methods and course content directly or indirectly addresses a number of core UNSW graduate capabilities, as follows

- Developing scholars who have a deep understanding of their discipline, through lectures and solution of analytical problems in tutorials and assessed by assignments and written examinations.
- Developing rigorous analysis, critique, and reflection, and ability to apply knowledge and skills to solving problems. These will be achieved by the laboratory experiments and interactive checkpoint assessments and lab exams during the labs.
- Developing capable independent and collaborative enquiry, through a series of tutorials spanning the duration of the course.
- Developing digital and information literacy and lifelong learning skills through assignment work.

Appendix C: Engineers Australia (EA) Competencies

Stage 1 Competencies for Professional Engineers

	Program Intended Learning Outcomes
PE1: Knowledge and Skill Base	PE1.1 Comprehensive, theory-based understanding of underpinning fundamentals
	PE1.2 Conceptual understanding of underpinning maths, analysis, statistics, computing
	PE1.3 In-depth understanding of specialist bodies of knowledge
	PE1.4 Discernment of knowledge development and research directions
	PE1.5 Knowledge of engineering design practice
	PE1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice
PE2: Engineering Application Ability	PE2.1 Application of established engineering methods to complex problem solving
	PE2.2 Fluent application of engineering techniques, tools and resources
	PE2.3 Application of systematic engineering synthesis and design processes
	PE2.4 Application of systematic approaches to the conduct and management of engineering projects
PE3: Professional and Personal Attributes	PE3.1 Ethical conduct and professional accountability
	PE3.2 Effective oral and written communication (professional and lay domains)
	PE3.3 Creative, innovative and pro-active demeanour
	PE3.4 Professional use and management of information
	PE3.5 Orderly management of self, and professional conduct
	PE3.6 Effective team membership and team leadership