School of Electrical Engineering and Telecommunications

Term 1, 2020

Course Outline

ELEC3106 Electronics

COURSE STAFF

Course Convener, Tutor: Torsten Lehmann Room EE-343 t.lehmann@unsw.edu.au
Laboratory Contact: Julian Keledjian

Consultations: You are encouraged to ask questions on the course material in class time, during the consultation time, or via Moodle rather than via email. *All* email enquiries should be made from your student email address with ELEC3106 in the subject line.

Keeping Informed: Announcements may be made during classes, and/or via online learning and teaching platforms – in this course, we will use Moodle https://moodle.telt.unsw.edu.au/login/index.php. Please note that you will be deemed to have received all announcements.

COURSE SUMMARY

Contact Hours

The course consists of 4 hours of lectures, a 1-hour tutorial, and 3 hours laboratory work each week. Laboratory sessions and tutorial classes start in week 1.

	Days	Time	Location
Lectures	Tue / Wed	3–5pm / 3-5pm	CLB-6 / CLB-6
Consultation	Tue / Wed	6–7pm / 5–6pm	EE-343 / EE-343
Tutorials	Tue / Wed	5–6pm / 1–2pm, 2–3pm	OMB-G32 / Quad-G034, LawTh-G23
Laboratories	Mon	9am–12pm, 2–5pm	EE-214, EE-G14
	Tue / Wed	9am–12pm, 12–3pm / 9am–12pm	EE-G14, EE-G14 / EE-214
	Thu	9am–12pm, 12–3pm, 3–6pm	EE-G14, EE-G14, EE-G14
	Fri	2–5pm	EE-G14

Public holiday class rescheduling: Fri wk8→Tue wk11; Mon wk9→Mon wk11.

Context and Aims

Physical electronic circuits and systems are plagued by a number of undesired effects that the designer need be aware of in order to implement operational electronics. Electrical noise and non-linearity, for instance, limit signal dynamic range; dynamic power supply currents can lead to corruption of digital data; electromagnetic interference (EMI) can cause system malfunction; parasitic components limit the operating frequencies of all circuits. Modern electronic systems, such as laptops and mobile phones, are actually extraordinarily difficult to implement. The *Electronics* course introduces you to a number of important undesired effects of electronic systems and ways to deal with these; also, it introduces some more advanced circuit functions.

Aims: The course aims to make you understand critical non-ideal effects in electronic devices and systems and how to address such effects, thus enabling you to design and construct physical electronic circuits that operate as desired.

Indicative Lecture Schedule

Period	Summary of Lecture Program	Reading Material
Week 1	Op-amp voltage/current limitations, offsets, biasing. CMRR, PSRR, parameter variation. Slew-rate, bandwidth, compensation. Distortion, saturation.	PW ch. 5, notes, datasheets
Week 2	Electrical noise. Dynamic range. Digital fan-out, noise margins. Logic families, VTC, I/O characteristics.	SS Ch. 15, PW ch. 6, notes, datasheets
Week 3	Gate delays, timing. Interfacing to logic, opto-coupling. Level-shifting, ESD. Driving transmission lines, human interfaces.	SS ch. 15, PW ch. 6+9, videos, datasheets
Week 4	Grounding, decoupling. Noise coupling, shielding. EMC, mixed A/D. **Quiz 1**.	PW ch. 1+8
Week 5	Power supplies, linear regulators, rectification. Switch-mode supplies, start-up. Batteries, solar cells. Thermal modelling.	PW ch. 7, ch. 9
Week 6	Flexibility week – no lectures.	
Week 7	SPICE simulations, models, functions. Simulation types and limitations. Power stages (A, B, AB, D). Protection, biasing.	Notes, SS ch. 11
Week 8	Filtering. Passive and active filters. Filter design, sensitivity. **Quiz 2**.	SS ch. 13
Week 9	Oscillators. Multipliers, Schmitt triggers, PLL. AGC, sensors, interfaces.	SS ch. 2+14
Week 10	Electronic failure mechanisms. Reliability. FMEA, watchdogs, defensive programming. **Guest**.	PW ch. 6+9, Notes

SS: Sedra & Smith; PW: P. Wilson

Indicative Laboratory and Tutorial Schedule

Period	Summary of Laboratory Program	Tutorial Program
Week 1	Lab 1: op-amp measurements.	Tute 1: op-amps.
Week 2	Lab 1 cont.	Tute Ex-2016-Q1.
Week 3	Lab 2: logic gate measurements. **Lab 1 report** due.	Tute 2: logic.
Week 4	Lab 2 cont.	Tute Ex-2016-Q2.
Week 5	Lab 3: PCB EMI measurements. **Lab 2 report** due.	Tute 3: power supplies.
Week 6	Design lab. Soldering workshop.	
Week 7	Lab 4: EMI simulations with SPICE. **Lab 3 report** due.	Tute Ex-2016-Q3.
Week 8	Design lab (Mon, Tue, Wed, Thu).	Tute 4: power amps.
Week 9	Design lab (Tue, Wed, Thu, Fri). **Lab 4 report** due.	Tute 5: filters & non-lin.
Week 10	Design demonstration (Tue, Wed) / Design lab (Mon, Fri).	Tute Ex-2016-Q4.
Week 11	Design demonstration (Mon, Fri). **Design lab report** due.	

Assessment

Laboratory work and report (labs 1–4)	15 %
Laboratory design task and report (lab 5)	15 %
Quizzes	10 %
Final Examination (2 hours)	60 % (exam mark $\geq$ 45 % required to pass course)

COURSE DETAILS

Credits

This is a 6 UoC course and the expected workload is 15 hours per week throughout the 10 week term.

Relationship to Other Courses

This is a 3rd year course in the School of Electrical Engineering and Telecommunications. It is a core course for students following a BE (Electrical) or (Telecommunications) program and other combined degree programs, and an elective for Computer Engineering students.

Pre-requisites and Assumed Knowledge

The pre-requisites for this course are ELEC2133, Analogue Electronics, and ELEC2141, Digital Circuit Design. ELEC2133 may be taken as a co-requisite. It is also required that you have good working knowledge of circuit theory and some basic signal analysis as covered in the courses ELEC1111, Electrical and Telecommunications Engineering, and ELEC2132 Circuits and Signals. It is finally assumed that you are proficient in the use of personal computers, and are able to operate electronics laboratory equipment independently.

Following Courses

The course is a pre-requisite for the fourth-year professional elective courses in the electronics area: ELEC4601, Digital and Embedded Systems Design, ELEC4602, Microelectronics Design and Technology, and ELEC4604, RF Electronics. These courses are again pre-requisites for post-graduate level courses in electronics.

Learning outcomes

After successful completion of this course, you should be able to:

1. identify critical non-ideal effects in analogue and digital electronic circuits,
2. appreciate the wealth of electronic circuit functions available,
3. appropriately design for EMC,
4. design simple power supplies and circuits,
5. interface analogue circuits and digital circuits,
6. design for failure protection in firmware and hardware, and
7. design electronic systems that work reliably.

This course is designed to provide the above learning outcomes which arise from targeted graduate capabilities listed in **Appendix A**. The targeted graduate capabilities broadly support the UNSW and Faculty of Engineering graduate capabilities (listed in **Appendix B**). This course also addresses the Engineers Australia (National Accreditation Body) Stage I competency standard as outlined in **Appendix C**.

Syllabus

Non-ideal effects in electronic circuits and systems: Noise; device noise, external noise, CMRR, PSRR, mixed A/D. Distortion; non-linearity, dynamic range, saturation. Stability and performance sensitivity to parameter variations. Some simple design for stability and performance. Design optimisation. Power-supply distribution and decoupling. Mixed analogue/digital system design, including grounding and shielding. Device modelling in SPICE. Data sheet interpretation. Design of analogue and digital circuits and system components: Non-linear circuits; oscillators, PLLs, multipliers, AGCs, Schmitt triggers. Introduction to filter design; active filters; op-amp. Sensors and actuators, PTAT; instrumentation amplifiers and signal conditioning. Low-level design and optimisation of digital CMOS gates. Gate delay, power dissipation, noise margins, fan-out. Introduction to integrated circuit design. Thermal consideration, power supplies, reliability, μC watchdogs

TEACHING STRATEGIES

Delivery Mode

- Formal face-to-face lectures, which provide you with a focus on the core analytical material in the course, together with qualitative, alternative explanations and individually targeted illustrations to aid your understanding;
- Tutorials, which allow for exercises in problem solving and allow time for you to resolve in-depth problems for quantitative understanding of the lecture material;
- Laboratory sessions, which experimentally support the formal lecture material and also provide you with practical design, construction, measurement and debugging skills.
- Design labs, which support creativity set in the course context solving an open-ended design problem with experimental verification.

Learning in this Course

You are expected to attend all lectures, tutorials, labs, and quizzes in order to maximise learning. You must prepare well for your laboratory classes and your lab work will be assessed. You should read relevant sections of the recommended texts. For most topics, lecture notes will not be given: reading and reflecting on the recommended texts and identify critical parts with the aid of the lectures is an essential component of this course. Reading additional texts will further enhance your learning experience. Group learning is also encouraged. UNSW assumes that self-directed study of this kind is undertaken in addition to attending face-to-face classes throughout the course.

Lectures

During the lectures technology capabilities and design issues are discussed and theoretical aspects of electronics design and technology are presented. Numerous examples of analogue and digital electronic circuit functions are discussed in order to convey a qualitative understanding of circuit operations, non-idealities, and EMI. You are encouraged to actively engage in the lectures to facilitate two-way communication and enhance learning. The lectures aim to support you in identifying and analysing non-ideal effects in circuits, to aid in learning how to mitigate such effects, and finally to help you appreciate the capabilities and limitations of the technology.

Tutorial Classes

You should attempt all of your problem sheet questions in advance of attending the tutorial classes. The importance of adequate preparation prior to each tutorial cannot be overemphasised, as the effectiveness and usefulness of the tutorial depends to a large extent on this preparation. Group learning is encouraged. Answers for these questions will be discussed during the tutorial class and the tutor will cover the more complex questions in the tutorial class.

Laboratory Program

The laboratory work provides you with hands-on experience in measuring non-ideal effects and EMI in electronic circuits, and thus helps to re-enforce the central topics in the course. Most of the laboratory work being carried out on bread boards constructed by you, also exercises your ability to set up measurements and locating circuit errors. The laboratory work will be carried out in groups of two students.

Laboratory Design Task

The design laboratory exercise is a small design task which aims to draw together theoretical and practical design aspects in a small open-ended design problem. You will design a circuit meeting given specifications during ther term and debug and characterise the circuit during the design laboratory sessions. The design task provide and test engineering creativity, open-ended problem solving skills, communication skills and general understanding of the course content.

ASSESSMENT

The assessment scheme in this course reflects the intention to assess your learning progress through the semester. Ongoing assessment occurs through the lab classes, lab reports, and class-time quizzes.

Laboratory Assessment

While laboratory work is primarily about learning, it is assessed to ensure that you understand the material in this essential course component. This assessment test that you can use the lab equipment, understand circuit models and non-idealities, carry out measurements, and can design simple circuits.

You are required to maintain a lab book for recording your observations and you must bring a camera or USB stick to capture CRO images of your observations for documentation. After completing each lab component, your work will be assessed by the laboratory demonstrator, so make sure that your demonstrator notice your work. Laboratory work must be documented in *brief* reports which are due Monday the week after the laboratory session ending each exercise. Late submissions carry a 50% penalty for the first week and will not be accepted beyond one week delay. Delays on medical grounds are accepted. Each report must be uploaded as a `.pdf` file (no other format accepted) on the course Moodle site.

Assessment marks (grade only) will be awarded according to how much of the lab you were able to complete, your understanding of the experiments conducted during the lab, and your ability to concisely express lab findings in your report. A HD mark is given only for exceptional performance that includes an attempt to complete any optional laboratory extensions; a serious attempt at completing the problems is required for a PS mark.

Laboratory Design Task Assessment

The design task is assessed to test your ability to design a simple electronic circuit, thus also demonstrating the your appreciation of the technology, and ability to use appropriate components and conduct suitable analysis to aid the design.

As for the other laboratory work, you are required to maintain a lab book and bring a camera or USB stick for recording your observations. Again, your work will be assessed by the laboratory demonstrator, so make sure that your demonstrator notice your work. The design and experimentation work must be documented in a *brief* report which is due Monday the week after the last design laboratory session. Late submissions carry a 50% penalty for the first week and will not be accepted beyond one week delay. Delays on medical grounds are accepted. Each report must be uploaded as a `.pdf` file (no other format accepted) on the course Moodle site.

Assessment marks (grade only) will be awarded according to your understanding of the design problem and experiments conducted during the lab, the quality and innovativeness of your design, and your ability to concisely explain and characterise your design in your report. A HD mark is given only for exceptional performance that includes functions exceeding the design requirements; a serious attempt at completing the problem is required for a PS mark.

Quizzes

There are two quizzes held during the lecture time through the semester. These are designed to give early feed-back on your progress through the theoretical components of the course and test your general understanding of the course material. Questions will be drawn from course material covered in the four weeks prior to each quiz. Assessment marks are given according the correct fraction of the answers to the quiz questions.

Final Examination

The exam in this course is a standard closed-book two-hour written examination. University approved calculators are allowed. The examination tests analytical and critical thinking and general understanding of the course material in a controlled fashion. Questions may be drawn from any aspect of the course (including laboratories), unless specifically indicated otherwise by the lecturer. Assessment marks will be assigned according to the correctness of the responses.

Relationship of Assessment Methods to Learning Outcomes

	Learning Outcomes						
Assessment	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Laboratory work and report			✓		✓		
Laboratory design task and report				✓			✓
Quizzes			✓		✓		
Final examination	✓	✓	✓		✓	✓	

COURSE RESOURCES

Textbooks

Prescribed textbook

- A. S. Sedra & K. C. Smith, *Microelectronic Circuits*. Oxford University Press, 7th ed., 2016.
- P. Wilson, *The Circuit Designer's Companion*. Elsevier, 3rd ed. 2012.

Note, if you use the 6th edition of SS, subtract 1 from the chapter references in the lecture schedule (except for chapter 2).

Reference books

- P. Horowitz & W. Hill, *The Art of Electronics*. Cambridge University Press, 3rd ed., 2015.
- E. Bogatin, *Signal and Power Integrity — Simplified*. Pearson, 2nd ed., 2009.

On-line resources

Moodle

As a part of the teaching component, Moodle will be used to upload lab reports and host forums. Lecture recordings will and assessment marks will also be made available via Moodle: https://moodle.telt.unsw.edu.au/login/index.php.

Course webpage

The course webpage is used to disseminate course material, including laboratory notes and design brief, past assessment and examination papers, and some lecture notes: https://subjects.ee.unsw.edu.au/elec3106.

OTHER MATTERS

Dates to note

Important dates are available at: https://student.unsw.edu.au/dates

Academic Honesty and Plagiarism

Plagiarism is the unacknowledged use of other people's work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a form of academic misconduct, and the University has very strict rules that include some severe penalties. For UNSW policies, penalties and

information to help you avoid plagiarism, see: https://student.unsw.edu.au/plagiarism. To find out if you understand plagiarism correctly, try this short quiz: https://student.unsw.edu.au/plagiarism-quiz.

Student Responsibilities and Conduct

You are expected to be familiar with and adhere to all UNSW policies (see https://student.unsw.edu.au/guide), and particular attention is drawn to the following:

Workload

It is expected that you will spend at least **15 hours per week** studying a 6 UoC course, from Week 1 until the final assessment, including both face-to-face classes and independent, self-directed study. In periods where you need to need to complete assignments or prepare for examinations, the workload may be greater. Over-commitment has been a common source of failure for many students. You should take the required workload into account when planning how to balance study with employment and other activities.

Attendance

Regular and punctual attendance at all classes is expected. UNSW regulations state that if students attend less than 80% of scheduled classes they may be refused final assessment.

General Conduct and Behaviour

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and students may be asked to leave the class.

Work Health and Safety

UNSW policy requires each person to work safely and responsibly, in order to avoid personal injury and to protect the safety of others.

Special Consideration and Supplementary Examinations

You must submit all assignments and attend all examinations scheduled for your course. As of Term 1 2019, assessment of applications for Special Consideration will be managed centrally and the University has introduced a “fit to sit/submit” rule. You will no longer be required to take your original documentation to The Nucleus for verification. Instead, UNSW will conduct source checks on documentation for verification purposes. You can apply for special consideration when illness or other circumstances beyond your control interfere with an assessment performance. If you need to submit an application for special consideration for an exam or assessment, you must submit the application **prior to the start** of the exam or before the assessment is submitted, except where illness or misadventure prevent you from doing so. If you sit an exam or submit an assignment, you are declaring yourself well enough to do so. For more detail, consult: https://student.unsw.edu.au/special-consideration.

Continual Course Improvement

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the myExperience process. You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings. As a result of previous feedback obtained for this course, and in our efforts to provide a rich and meaningful learning experience, we have changed the weighting of in-semester assessments, increased the number of tutorial exercises, commenced use of the LTSpice simulator program, provided supplementary lecture notes on selected topics, released lecture summary slides, and provided lecture video recordings.

Administrative Matters

On issues and procedures regarding such matters as special needs, equity and diversity, occupational health and safety, enrolment, rights, and general expectations of students, please refer to the School and UNSW policies: https://www.engineering.unsw.edu.au/electrical-engineering/resources/ and https://student.unsw.edu.au/guide.

APPENDICES

Appendix A: Targeted Graduate Capabilities

Electrical Engineering and Telecommunications programs are designed to address the following targeted capabilities which were developed by the school in conjunction with the requirements of professional and industry bodies:

- The ability to apply knowledge of basic science and fundamental technologies;
- The skills to communicate effectively, not only with engineers but also with the wider community;
- The capability to undertake challenging analysis and design problems and find optimal solutions;
- Expertise in decomposing a problem into its constituent parts, and in defining the scope of each part;
- A working knowledge of how to locate required information and use information resources to their maximum advantage;
- Proficiency in developing and implementing project plans, investigating alternative solutions, and critically evaluating differing strategies;
- An understanding of the social, cultural and global responsibilities of the professional engineer;
- The ability to work effectively as an individual or in a team;
- An understanding of professional and ethical responsibilities;
- The ability to engage in lifelong independent and reflective learning.

Appendix B: UNSW Graduate Capabilities

The course delivery methods and course content directly or indirectly addresses a number of core UNSW graduate capabilities, as follows:

- Developing rigorous analysis, critique, and reflection, and ability to apply knowledge and skills to solving problems, through laboratory experiments and tutorial exercises.
- Developing capable independent and collaborative enquiry, through tutorials exercises.
- Developing digital and information literacy and lifelong learning skills, through lectures, class preparations and report writing.
- Developing the capability of effective communication, through report writing.
- Developing independent, self-directed professionals who are enterprising, innovative, creative and responsive to change, through the design task.

Appendix C: Engineers Australia (EA) Professional Engineer Competency Standard

	Program Intended Learning Outcomes	
PE1: Knowledge and Skill Base	PE1.1 Comprehensive, theory-based understanding of underpinning fundamentals	✓
	PE1.2 Conceptual understanding of underpinning maths, analysis, statistics, computing	✓
	PE1.3 In-depth understanding of specialist bodies of knowledge	✓
	PE1.4 Discernment of knowledge development and research directions	
	PE1.5 Knowledge of engineering design practice	✓
	PE1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice	
PE2: Engineering Application Ability	PE2.1 Application of established engineering methods to complex problem solving	✓
	PE2.2 Fluent application of engineering techniques, tools and resources	✓
	PE2.3 Application of systematic engineering synthesis and design processes	
	PE2.4 Application of systematic approaches to the conduct and management of engineering projects	
PE3: Professional and Personal Attributes	PE3.1 Ethical conduct and professional accountability	
	PE3.2 Effective oral and written communication (professional and lay domains)	✓
	PE3.3 Creative, innovative and pro-active demeanour	✓
	PE3.4 Professional use and management of information	✓
	PE3.5 Orderly management of self, and professional conduct	✓
	PE3.6 Effective team membership and team leadership	