School of Electrical Engineering and Telecommunications

Term 3, 2019

Course Outline

ELEC4602
Microelectronics Design & Technology

COURSE STAFF

Course Convener: Torsten Lehmann Room EE-343 t.lehmann@unsw.edu.au

Laboratory Contact: Edward Yang

Consultations: You are encouraged to ask questions on the course material in class time, during the consultation time, or via Moodle rather than via email. *All* email enquiries should be made from your student email address with ELEC4602 in the subject line.

Keeping Informed: Announcements may be made during classes, and/or via online learning and teaching platforms – in this course, we will use Moodle https://moodle.telt.unsw.edu.au/login/index.php. Please note that you will be deemed to have received all announcements.

COURSE SUMMARY

Contact Hours

The course consists of 3 hours of lectures, a 3-hour laboratory session and a 1-hour tutorial each week. Laboratory sessions start in week 1, tutorial classes start in week 2.

	Days	Time	Location
Lectures	Tuesdays	3–6pm	CLB-1
Consultation	Thursdays / Fridays	5–6pm / 1–2pm	EE-343
Tutorials	Thursdays Fridays	4–5pm 12–1pm	Ainswth-G01 EE-G09
Laboratories	Thursdays Fridays	1–4pm 9am–12pm	EE-108 EE-108

Context and Aims

Microelectronics or integrated electronics is the miniaturised electronic circuits that make up Integrated Circuits (ICs) such as microprocessors, Field-Programmable Gate Arrays, Flash-memories, operational amplifier, analogue-to-digital converters and many other functions. Most ICs today are implemented in various flavours of CMOS technology which is the focus of this course. The ability to use large number of components at relative low cost and the ability to match components accurately on-chip makes the design of integrated circuits and systems different from a similar design using discrete components. *Microelectronics Design and Technology* is a broad based, introductory IC design course, which takes the student through all the necessary steps in order to complete (ready-to-manufacture) a basic mixed-signal front-end in a typical integrated system.

Aims: The course aims to make the student familiar with CMOS microelectronics technologies, and enable the student to do analysis and design of circuits implemented in these technologies.

Indicative Lecture Schedule

Period	Summary of Lecture Program	Reading Material
Week 1	CMOS processing technologies and components. Layout layers.	JB ch. 7, web, JB ch. 3, 4, 5.
Week 2	IC layout and design rules. Design Synthesis and verification tools.	JB ch. 3, 4, web.
Week 3	Analogue and digital MOS models and device noise.	JB ch. 9, 10, JB ch. 8.
Week 4	Single-stage amplifiers. **Quiz 1**.	JB ch. 20, 21, 22.
Week 5	Operational amplifier design. Comparators.	JB ch. 24, 27.
Week 6	Samplers and charge injection. Data converter metrics.	JB ch. 25, JB ch. 28.
Week 7	D/A and A/D converter design.	JB ch. 29.
Week 8	CMOS inverters and logic. **Quiz 2**.	JB ch. 11.
Week 9	Static CMOS logic design. Sequential CMOS logic.	JB ch. 12, 13.
Week 10	Dynamic CMOS logic. Memory design and topologies.	JB ch. 14, 16.

JB: J. Baker

Indicative Laboratory and Tutorial Schedule

Period	Summary of Laboratory Program	Tutorial Program
Week 1	Lab 1: layout.	No tute.
Week 2	Lab 1 cont.	Tute 1: layout..
Week 3	Lab 2: circuit simulation. **Lab 1 report** due.	Tute 2: transistor models.
Week 4	Lab 2 cont. Project	Tute 3: single-stage amplifiers.
Week 5	Lab 3: op-amp design. Project **Lab 2 report** due.	Tute 4: op-amps.
Week 6	Lab 3 cont. Project	Tute 5: sampling & comparators.
Week 7	Lab 4: combinational logic. Project **Lab 3 report** due.	Tute 6: ADC converters.
Week 8	Lab 4 cont. Project	Tute 7: CMOS inverters.
Week 9	Lab 5: sequential logic. Project **Lab 4 report** due.	Tute 8: CMOS logic.
Week 10	Lab 5 cont. **Project report** due.	Tute 9: sequential logic.
Week 11	**Lab 5 report** due.	

Assessment

Laboratory work and report (labs 1–5)	15 %
Project design task and report	15 %
Quizzes	10 %
Final Examination (2 hours)	60 % (exam mark $\geq 45\%$ required to pass course)

COURSE DETAILS

Credits

This is a 6 UoC course and the expected workload is 15 hours per week throughout the 10 week term.

Relationship to Other Courses

This is a 4th year course in the School of Electrical Engineering and Telecommunications. It is a professional elective course for students following a BE (Electrical) or (Telecommunications) program and other combined degree programs.

Pre-requisites and Assumed Knowledge

The pre-requisite for this course is ELEC3106, Electronics. It is essential that you have good working knowledge of circuit theory, basic analogue and digital electronics, and basic signal analysis as covered in the courses ELEC1112, Electrical Circuits, ELEC2133, Analogue Electronics, ELEC2141, Digital Circuit Design, and ELEC2134, Circuits and Signals. It is finally assumed that you are proficient in the use of personal computers.

Following Courses

The course is a co-requisite for the post-graduate course ELEC9701, Mixed Signal Microelectronics Design. The course is also a co-requisite for thesis work in the area of integrated circuit design.

Learning outcomes

After successful completion of this course, you should be able to:

1. appreciate capabilities and limitations of current microelectronic (or IC) technologies,
2. use modern CAD design tools to design ICs,
3. create IC layouts,
4. understand and use circuit models of IC components,
5. analyse simple analogue and digital microelectronic circuits, and
6. design simple analogue, digital and mixed microelectronic circuits.

This course is designed to provide the above learning outcomes which arise from targeted graduate capabilities listed in **Appendix A**. The targeted graduate capabilities broadly support the UNSW and Faculty of Engineering graduate capabilities (listed in **Appendix B**). This course also addresses the Engineers Australia (National Accreditation Body) Stage I competency standard as outlined in **Appendix C**.

Syllabus

Basic IC processing technology: lithography, oxidation, diffusion, implantation, film deposition, etching, metalisation. IC layout, layout layers and functions, design rules, scaling. Design synthesis and verification tools, p-cells, cell libraries, place-and-route, HDL compilers, layout-versus-schematic, circuit simulators. Analogue and digital MOS device models. On-chip components: capacitors, inductors, resistors, diodes. Floor planing, cell layout and routing. Corner and Monto Carlo simulations. CMOS analogue building blocks: current mirrors, differential stage, active load, single-stage amplifiers. Noise sources and analysis. CMOS operational amplifier design, frequency compensation, output stages. D/A converters and A/D converters. Ring oscillators. Static CMOS gates and flip-flops, transmission gates. CMOS digital building blocks: level shifters, decoders, multiplexers, tri-states, buffers. Gate timing. Memories: ROM, SRAM and DRAM cell design; sense amplifiers.

TEACHING STRATEGIES

Delivery Mode

- Formal face-to-face lectures, which provide you with a focus on the core analytical material in the course, together with qualitative, alternative explanations and individually targeted illustrations to aid your understanding;
- Tutorials, which allow for exercises in problem solving and allow time for you to resolve in-depth problems for quantitative understanding of the lecture material;
- Computer laboratory sessions, which support, via detailed simulations using state-of-the art CAD tools, the formal lecture material and also provide you with practical design, and debugging skills;
- A design task, which draws together theoretical and practical design aspects in an open-ended realistic design problem, reinforcing the course material.

Learning in this Course

You are expected to attend all lectures, labs, and quizzes, as well as completing the tutorials, in order to maximise your learning. You must prepare well for your laboratory classes and your lab work will be assessed. You should read relevant sections of the recommended texts. For most topics, lecture notes will not be given: reading and reflecting on the recommended texts and identify critical parts with the aid of the lectures is an essential component of this course. Reading additional texts will further enhance your learning experience. Group learning is also encouraged. UNSW assumes that self-directed study of this kind is undertaken in addition to attending face-to-face classes throughout the course.

Lectures

During the lectures technology capabilities and design issues are discussed and theoretical aspects of IC design and technology are presented. Numerous examples of analogue and digital integrated circuit functions are discussed in order to convey a qualitative understanding of circuit operations. You are encouraged to actively engage in the lectures to facilitate two-way communication and enhance learning. The lectures aim to support you in analysing and designing integrated circuits, and to help you appreciate the capabilities of IC technologies.

Tutorial Classes

You should attempt all of your problem sheet questions in advance of attending the tutorial classes. The importance of adequate preparation prior to each tutorial cannot be overemphasised, as the effectiveness and usefulness of the tutorial depends to a large extent on this preparation. Group learning is encouraged. Answers for these questions will be discussed during the tutorial class and the tutor will cover the more complex questions in the tutorial class.

Laboratory Program

The laboratory work provides you with hands-on design experience and exposure to state-of-the-art CAD tools. The laboratory thus enables you to use these tools for IC circuit design, analysis and lay-out, and re-enforces the central topics in the course. Verifying circuit functions by simulations also train you in best-practice IC verification and exercises your ability to locate circuit errors.

Design Task

The design task aims to draw together theoretical and practical design aspects in an open-ended realistic design problem. You will design an integrated circuit meeting given specifications, use the CAD tools to verify the circuit operation and write a report documenting your design. The design task provide and test engineering creativity, open-ended problem solving skills, communication skills and general understanding of the course content. You may use the CAD tools in rooms EE-202/EE-209/EE-217 for this task. You may also use up to 1 h/week of the scheduled laboratory time for the design task where demonstrators can assist you.

ASSESSMENT

The assessment scheme in this course reflects the intention to assess your learning progress through the semester. Ongoing assessment occurs through the lab classes, lab reports, and class-time quizzes.

Laboratory Assessment

While laboratory work is primarily about learning, it is assessed to ensure that you understand the material in this essential course component. This assessment test that you can use the CAD tools, create IC layouts, understand circuit models and functions, carry out appropriate simulations, and can design simple circuits.

You are required to maintain a lab book for recording your observations and you must bring a USB stick to capture screen shots or print-outs of your work for documentation. After completing each key lab component, your work will be assessed by the laboratory demonstrator, so make sure that your demonstrator notice your work. Laboratory work must be documented in *brief* reports which are due *Monday* the week after the laboratory session ending each exercise. Late submissions carry a 50% penalty for the first week and will not be accepted beyond one week delay. Delays on medical grounds are accepted. Each report must be uploaded as a `.pdf` file (no other format accepted) on the course Moodle site.

Assessment marks (grade only) will be awarded according to how much of the lab you were able to complete, your understanding of the work conducted during the lab, and your ability to concisely express lab findings in your report. A HD mark is given only for exceptional performance that includes an attempt to complete any laboratory extensions; a serious attempt at completing the problems is required for a PS mark.

Design Task Assessment

The design task is assessed to test your ability to design a simple integrated circuit, thus also demonstrating your appreciation of the technology, your ability to use appropriate models and simulations, and your ability to conduct suitable analysis to aid in the design.

As for the other laboratory work, you should maintain a lab book and must record suitable screen shots or print-outs as documentation for your work. The design and verification work must be documented in a *brief* report which is due *Monday* the due week listed in the laboratory schedule. Late submissions carry a 50% penalty for the first week and will not be accepted beyond one week delay. Delays on medical grounds are accepted. Each report must be uploaded as a `.pdf` file (no other format accepted) on the course Moodle site.

Assessment marks (grade only) will be awarded on the basis of your report according to your understanding of the design problem, simulations carried out, the quality and innovativeness of your design, and your ability to concisely explain and characterise your design in your report. A HD mark is given only for exceptional performance that exceed design requirements; a serious attempt at completing the problem is required for a PS mark.

Quizzes

There are two quizzes held during the lecture time through the semester. These are designed to give early feed-back on your progress through the theoretical components of the course and test your general understanding of the course material. Questions will be drawn from course material covered in the four weeks prior to each quiz. Assessment marks are given according the correct fraction of the answers to the quiz questions.

Final Examination

The exam in this course is a standard closed-book 2 hour written examination. University approved calculators are allowed. The examination tests analytical and critical thinking and general understanding of the course material in a controlled fashion. Questions may be drawn from any aspect of the course (including

laboratories), unless specifically indicated otherwise by the lecturer. Assessment marks will be assigned according to the correctness of the responses. An examination mark of at least 45% is required to pass the course.

Relationship of Assessment Methods to Learning Outcomes

	Learning Outcomes					
Assessment	**1**	**2**	**3**	**4**	**5**	**6**
Laboratory work and report	✓	✓	✓			
Design task and report	✓	✓		✓		✓
Quizzes				✓	✓	
Final examination	✓		✓	✓	✓	✓

COURSE RESOURCES

Textbooks

Prescribed textbook

- R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*. Wiley Interscience, 2nd/3rd ed., 2005/2010.

Reference books

- T. C. Carusone, D. A. Johns and K. W. Martin, *Analog Integrated Circuit Design*. Wiley and Sons Inc., 2nd ed., 2012.
- T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 1998.
- N. Weste and D. Harris, *CMOS VLSI Design: a Circuits and Systems Perspective*. Addison-Wesley, 3rd ed., 2005.

On-line resources

Moodle

As a part of the teaching component, Moodle will be used to upload lab reports and host forums. Assessment marks will also be made available via Moodle: https://moodle.telt.unsw.edu.au/login/index.php.

Course webpage

The course webpage is used to disseminate course material, including laboratory notes and design brief, past assessment and examination papers, and some lecture notes: https://subjects.ee.unsw.edu.au/elec4602.

CAD resources

Students will use the PCs in the Signal Processing Laboratory EE-108 for all laboratory works. The CAD tools used in this course is the industry standard Cadence design suite which run under the Linux system Virtual Machine on the lab PCs. For specific details on how to log on, see the course web page. Students can access the CAD tools after hours on the PCs in the school located in rooms EE-202 and EE-217 as well as the open space area EE-209.

OTHER MATTERS

Dates to note

Important dates are available at: https://student.unsw.edu.au/dates

Academic Honesty and Plagiarism

Plagiarism is the unacknowledged use of other people's work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a form of academic misconduct, and the University has very strict rules that include some severe penalties. For UNSW policies, penalties and information to help you avoid plagiarism, see: https://student.unsw.edu.au/plagiarism. To find out if you understand plagiarism correctly, try this short quiz: https://student.unsw.edu.au/plagiarism-quiz.

Student Responsibilities and Conduct

You are expected to be familiar with and adhere to all UNSW policies (see https://student.unsw.edu.au/guide), and particular attention is drawn to the following:

Workload

It is expected that you will spend at least **15 hours per week** studying a 6 UoC course, from Week 1 until the final assessment, including both face-to-face classes and independent, self-directed study. In periods where you need to need to complete assignments or prepare for examinations, the workload may be greater. Over-commitment has been a common source of failure for many students. You should take the required workload into account when planning how to balance study with employment and other activities.

Attendance

Regular and punctual attendance at all classes is expected. UNSW regulations state that if students attend less than 80% of scheduled classes they may be refused final assessment.

General Conduct and Behaviour

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and students may be asked to leave the class.

Work Health and Safety

UNSW policy requires each person to work safely and responsibly, in order to avoid personal injury and to protect the safety of others.

Special Consideration and Supplementary Examinations

You must submit all assignments and attend all examinations scheduled for your course. You can apply for special consideration when illness or other circumstances beyond your control interfere with an assessment performance. If you need to submit an application for special consideration for an exam or assessment, you must submit the application **prior to the start** of the exam or before the assessment is submitted, except where illness or misadventure prevent you from doing so. Be aware of the "fit to sit/submit" rule which means that if you sit an exam or submit an assignment, you are declaring yourself well enough to do so and cannot later apply for Special Consideration. For more information and how to apply, see https://student.unsw.edu.au/special-consideration.

Continual Course Improvement

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the Course and Teaching Evaluation and Improvement Process. You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings. As a result of previous feedback obtained for this course, and in our efforts to provide a rich and meaningful learning experience, we have changed the weighting of in-semester assessments, introduced formal tutorial classes, and released summary slides.

Administrative Matters

On issues and procedures regarding such matters as special needs, equity and diversity, occupational health and safety, enrolment, rights, and general expectations of students, please refer to the School and UNSW policies: http://www.engineering.unsw.edu.au/electrical-engineering/resources and https://student.unsw.edu.au/guide.

APPENDICES

Appendix A: Targeted Graduate Capabilities

Electrical Engineering and Telecommunications programs are designed to address the following targeted capabilities which were developed by the school in conjunction with the requirements of professional and industry bodies:

- The ability to apply knowledge of basic science and fundamental technologies;
- The skills to communicate effectively, not only with engineers but also with the wider community;
- The capability to undertake challenging analysis and design problems and find optimal solutions;
- Expertise in decomposing a problem into its constituent parts, and in defining the scope of each part;
- A working knowledge of how to locate required information and use information resources to their maximum advantage;
- Proficiency in developing and implementing project plans, investigating alternative solutions, and critically evaluating differing strategies;
- An understanding of the social, cultural and global responsibilities of the professional engineer;
- The ability to work effectively as an individual or in a team;
- An understanding of professional and ethical responsibilities;
- The ability to engage in lifelong independent and reflective learning.

Appendix B: UNSW Graduate Capabilities

The course delivery methods and course content directly or indirectly addresses a number of core UNSW graduate capabilities, as follows:

- Developing rigorous analysis, critique, and reflection, and ability to apply knowledge and skills to solving problems, through laboratory experiments and tutorial exercises.
- Developing capable independent and collaborative enquiry, through tutorials exercises.
- Developing digital and information literacy and lifelong learning skills, through lectures, class preparations and report writing.
- Developing the capability of effective communication, through report writing.
- Developing independent, self-directed professionals who are enterprising, innovative, creative and responsive to change, through the design task.

Appendix C: Engineers Australia (EA) Professional Engineer Competency Standard

	Program Intended Learning Outcomes	
PE1: Knowledge and Skill Base	PE1.1 Comprehensive, theory-based understanding of underpinning fundamentals	✓
	PE1.2 Conceptual understanding of underpinning maths, analysis, statistics, computing	✓
	PE1.3 In-depth understanding of specialist bodies of knowledge	✓
	PE1.4 Discernment of knowledge development and research directions	✓
	PE1.5 Knowledge of engineering design practice	✓
	PE1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice	
PE2: Engineering Application Ability	PE2.1 Application of established engineering methods to complex problem solving	✓
	PE2.2 Fluent application of engineering techniques, tools and resources	✓
	PE2.3 Application of systematic engineering synthesis and design processes	✓
	PE2.4 Application of systematic approaches to the conduct and management of engineering projects	
PE3: Professional and Personal Attributes	PE3.1 Ethical conduct and professional accountability	
	PE3.2 Effective oral and written communication (professional and lay domains)	✓
	PE3.3 Creative, innovative and pro-active demeanour	✓
	PE3.4 Professional use and management of information	✓
	PE3.5 Orderly management of self, and professional conduct	✓
	PE3.6 Effective team membership and team leadership	