School of Electrical Engineering and Telecommunications

Semester 2, 2018
Course Outline

ELEC 4601
Digital and Embedded System Design

COURSE STAFF

Course Convener: Dr. Chamith Wijenayake, Hilmer building - room 643A, c.wijenayake@unsw.edu.au

Laboratory Contact: Mr Gajan Suthokumar, g.suthokumar@unsw.edu.au

Consultations: You are encouraged to ask questions on the course material, after the lecture class times in the first instance, rather than via email. Lecturer consultation time for this course will be on every **Thursday 4-6 pm** at Hilmer building room 643A. ALL email enquiries should be made from your student email address with ELEC4601 in the subject line; otherwise they will not be answered.

Keeping Informed: Announcements may be made during classes, via email (to your student email address) and/or via online learning and teaching platforms – in this course, we will use Moodle https://moodle.telt.unsw.edu.au/login/index.php. Please note that you will be deemed to have received this information, so you should take careful note of all announcements.

COURSE SUMMARY

Contact Hours

The course consists of 3 hours of lectures and a 3-hour laboratory session each week. **Laboratory sessions will start in week 4.**

	Day	Time	Location
Lectures	Monday	9am – 11am	Quad G045
	Wednesday	3pm – 4pm	BUS216
Laboratories	Monday	12pm – 3pm	ElecEngG14
	Monday	3pm – 6pm	ElecEngG14
Consultation	Thursday	4pm – 6pm	Hilmer 643A

Context and Aims

The objective of this course is to equip students with the concepts and skills that enable them to design advanced digital systems on programmable digital platforms such as FPGAs with a special emphasis on implementation of DSP systems. The course will cover a range of fast algorithms and digital design concepts used to develop area, speed and power optimized digital designs and will introduce students to a variety of rapid prototyping and high-level synthesis tools in addition to standard hardware description language (HDL) based system design.

Indicative Lecture/Laboratory Schedule

Week	Topic/Lecture	Lab
1	Introduction and data-flow representations	
2	Pipelining and parallel processing of feed-forward structures	
3	Register re-timing	
4	Unfolding and folding transformations	0
5	One and multidimensional systolic array design	1
6	One and multidimensional systolic array design	2
7	Pipelining and parallel processing of recursive structures	3
8	Pipelining and parallel processing of recursive structures	4
9	**Mid-session exam** (material up to end of week 6).	5
Mid-session break		
10	Introduction to wave-digital filter implementations	6
11	Fast algorithms and their implementations	7
12	Bit-level arithmetic architectures. Industry guest lecture (TBC)	8
13	Review.	

Laboratory activities

Labs will be conducted in a semi-guided and a case-study format where students will be required to verify certain theoretical concepts taught in the lectures through hardware/software prototyping. Students are required to submit a 2-4 page written report after each lab experiment explaining their findings and conclusions. Format and content of such lab reports will be discussed during the class.

Assessment

Laboratory case studies	30%
Mid-Semester Exam	10%
Homework problems	10%
Final Exam (2 hours)	50%

COURSE DETAILS

Credits

This is a 6 UoC course and the expected workload is 10–12 hours per week throughout the 13-week semester.

Relationship to Other Courses

This is a 4th year course in the School of Electrical Engineering and Telecommunications. It is an elective subject for students following a BE (Electrical) or (Telecommunications) program.

Pre-requisites and Assumed Knowledge

The pre-requisite for this course is ELEC2141 (Digital Circuit Design), ELEC 2142 (Embedded System Design) and ELEC 3104 (Digital Signal Processing). The fundamental knowledge for this course is based on the aforementioned pre-requisites. Students should have a good understanding of basic digital logic design concepts and fundamentals of digital signal processing.

Following Courses

N/A.

Learning outcomes

After the successful completion of the course, the student will be able to:

1. Understand a range of digital system implementation and optimizations schemes.
2. Develop speed, throughput, and power optimised custom hardware architectures for DSP.
3. Understand constraints and challenges in real-time digital systems and apply design techniques to overcome them.
4. Design and develop digital hardware architectures using a variety of tools including high-level synthesis and rapid FPGA prototyping.

This course is designed to provide the above learning outcomes, which arise from targeted, graduate capabilities listed in ***Appendix A***. The targeted graduate capabilities broadly support the UNSW and Faculty of Engineering graduate capabilities (listed in ***Appendix B***). This course also addresses the Engineers Australia (National Accreditation Body) Stage I competency standard as outlined in ***Appendix C***.

Syllabus

Data-flow representations, pipelining and parallel processing architectures for feed-forward data-flow structures, pipelining and parallel processing architectures for recursive data-flow structures, register retiming and optimisation for critical paths, unfolding and folding transformation and throughput enhancement, one and multidimensional systolic array design for massively parallel digital hardware designs, introduction to wave-digital filter based hardware implementations and sensitivity to parameter perturbations, fast algorithms for DSP and their digital hardware implementations, bit-level arithmetic architectures for digital VLSI.

TEACHING STRATEGIES

Delivery Mode

Teaching in this course aims at establishing a good fundamental understanding of the areas covered using:

- Formal face-to-face lectures, which provide you with a focus on the core analytical material in the course, together with qualitative, alternative explanations to aid your understanding;
- Laboratory sessions, which support the formal lecture material and also provide you with practical construction, measurement and debugging skills;

Regular homework problems will be released and will be graded and this keeps you up to date with the lecture material.

Learning in this course

You are expected to attend all lectures and labs, and mid-semester exams in order to maximise learning. You must prepare well for your laboratory classes and your lab work will be assessed. In addition to the lecture notes/video, you should read relevant sections of the recommended text. Reading additional texts will further enhance your learning experience. Group learning is also encouraged. UNSW *assumes* that self-directed study of this kind is undertaken in addition to attending face-to-face classes throughout the course.

Laboratory program

The laboratory experiments will be conducted in a semi-guided and a case-study format where students are asked to verify various design techniques taught in the lectures using Xilinx Vivado design suite (system edition). Labs start in week 4 and there will be 7-8 such lab activities. After each lab students are required to submit a 2-4 page written report explaining their implementations, results, and conclusions drawn. Any instance of clear plagiarism will result in zero mark for the entire laboratory component. **Laboratory attendance WILL be kept, and you MUST attend at least 80% of the labs to pass the course.**

Laboratory Exemption

There is no laboratory exemption for this course. Regardless of whether equivalent labs have been completed in previous courses, all students enrolled in this course must take the labs. If, for medical reasons, (note that a valid medical certificate must be provided) you are unable to attend a lab, you will need to apply for a catch-up lab during another lab time, as agreed by the laboratory coordinator.

ASSESSMENT

The assessment scheme in this course reflects the intention to assess your learning progress through the semester and will have the following breakdown.

Laboratory case studies	30%
Mid-semester exam	10%
Homework problems	10%
Final exam (2 hours)	50%

Laboratory Assessment

Students are required to submit a 2-4 page written report for each lab experiment, which includes any results obtained during the lab activities. Lab assessment is individual and is based on this lab report. Any instance of clear plagiarism will result in zero mark for the entire laboratory component.

Mid-Semester Exam

The mid-session examination tests your general understanding of the course material, and is designed to give you feedback on your progress through the analytical components of the course. Questions may be drawn from any course material up to the end of week 6. It may contain questions requiring some (not extensive) knowledge of laboratory material, and will definitely contain numerical and analytical questions. The mid-session exam will be held in week 9 (17/09/2018 9-11am).

Homework Problems

Regular homework problems will be released and will be used to keep the students up to date with the material. Students are required to submit written answers by the due date mentioned in each problem set.

Final Exam

The exam in this course is a standard closed-book 2-hour written examination, comprising 4 or 5 compulsory questions. University approved calculators are allowed. The examination tests analytical and critical thinking and general understanding of the course material in a controlled fashion. Questions may be drawn from any aspect of the course (including laboratory), unless specifically indicated otherwise by the lecturer. Marks will be assigned according to the correctness of the responses. *Please note that* ***you must pass the final exam in order to pass the course****.*

Relationship of Assessment Methods to Learning Outcomes

Assessment	Learning Outcomes			
	1	2	3	4
Labs	✓	✓	✓	✓
Mid-semester exam	✓		✓	
Homework	✓	✓	✓	✓
Final exam	✓	✓	✓	✓

COURSE RESOURCES

Textbooks

Prescribed textbook: VLSI Digital Signal Processing Systems: Design and Implementation, by Keshab K. Parhi, ISBN 0471241865, 9780471241867

On-line resources

Moodle

As a part of the teaching component, Moodle will be used to disseminate teaching materials, host forums and occasionally quizzes. Assessment marks will also be made available via Moodle: https://moodle.telt.unsw.edu.au/login/index.php.

Mailing list

Announcements concerning course information will be given in the lectures and/or on Moodle and/or via email (which will be sent to your student email address).

OTHER MATTERS

Dates to note

Important Dates available at: https://student.unsw.edu.au/dates

Academic Honesty and Plagiarism

Plagiarism is the unacknowledged use of other people's work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a form of academic misconduct, and the University has very strict rules that include some severe penalties. For UNSW policies, penalties and information to help you avoid plagiarism see https://student.unsw.edu.au/plagiarism. To find out if you understand plagiarism correctly, try this short quiz: https://student.unsw.edu.au/plagiarism-quiz.

Student Responsibilities and Conduct

Students are expected to be familiar with and adhere to all UNSW policies (see https://student.unsw.edu.au/guide), and particular attention is drawn to the following:

Workload

It is expected that you will spend at least **ten to twelve hours per week** studying a 6 UoC course, from Week 1 until the final assessment, including both face-to-face classes and *independent, self-directed study*. In periods where you need to need to complete assignments or prepare for examinations, the workload may be greater. Over-commitment has been a common source of failure for many students. You should take the required workload into account when planning how to balance study with employment and other activities.

Attendance

Regular and punctual attendance at all classes is expected. UNSW regulations state that if students attend less than 80% of scheduled classes they may be refused final assessment.

General Conduct and Behaviour

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and students may be asked to leave the class.

Work Health and Safety

UNSW policy requires each person to work safely and responsibly, in order to avoid personal injury and to protect the safety of others.

Special Consideration and Supplementary Examinations

You must submit all assignments and attend all examinations scheduled for your course. You should seek assistance early if you suffer illness or misadventure, which affects your course progress. All applications for special consideration must be **lodged online through myUNSW within 3 working days of the assessment**, not to course or school staff. For more detail, consult https://student.unsw.edu.au/special-consideration.

Continual Course Improvement

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the online student survey myExperience. You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings. As a result of previous feedback obtained for this course and in our efforts to provide a rich and meaningful learning experience, we have continued to evaluate and modify our delivery and assessment methods including revised lecture notes, tutorials, blended learning resources, in-class demonstrations, and industry guest lectures.

Administrative Matters

On issues and procedures regarding such matters as special needs, equity and diversity, occupational health and safety, enrolment, rights, and general expectations of students, please refer to the School and UNSW policies:
https://student.unsw.edu.au/guide
https://www.engineering.unsw.edu.au/electrical-engineering/resources

APPENDICES

Appendix A: Targeted Graduate Capabilities

Electrical Engineering and Telecommunications programs are designed to address the following targeted capabilities which were developed by the school in conjunction with the requirements of professional and industry bodies:

- The ability to apply knowledge of basic science and fundamental technologies;
- The skills to communicate effectively, not only with engineers but also with the wider community;
- The capability to undertake challenging analysis and design problems and find optimal solutions;
- Expertise in decomposing a problem into its constituent parts, and in defining the scope of each part;
- A working knowledge of how to locate required information and use information resources to their maximum advantage;
- Proficiency in developing and implementing project plans, investigating alternative solutions, and critically evaluating differing strategies;
- An understanding of the social, cultural and global responsibilities of the professional engineer;
- The ability to work effectively as an individual or in a team;
- An understanding of professional and ethical responsibilities;
- The ability to engage in lifelong independent and reflective learning.

Appendix B: UNSW Graduate Capabilities

The course delivery methods and course content directly or indirectly addresses a number of core UNSW graduate capabilities, as follows

- Developing scholars who have a deep understanding of their discipline, through lectures and solution of analytical problems in tutorials and assessed by assignments and written examinations.
- Developing rigorous analysis, critique, and reflection, and ability to apply knowledge and skills to solving problems. These will be achieved by the laboratory experiments and interactive checkpoint assessments and lab exams during the labs.
- Developing capable independent and collaborative enquiry, through a series of tutorials spanning the duration of the course.
- Developing digital and information literacy and lifelong learning skills through assignment work.

Appendix C: Engineers Australia (EA) Professional Engineer Competency Standard

	Program Intended Learning Outcomes	
PE1: Knowledge and Skill Base	PE1.1 Comprehensive, theory-based understanding of underpinning fundamentals	✓
	PE1.2 Conceptual understanding of underpinning maths, analysis, statistics, computing	✓
	PE1.3 In-depth understanding of specialist bodies of knowledge	✓
	PE1.4 Discernment of knowledge development and research directions	✓
	PE1.5 Knowledge of engineering design practice	✓
	PE1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice	
PE2: Engineering Application Ability	PE2.1 Application of established engineering methods to complex problem solving	✓
	PE2.2 Fluent application of engineering techniques, tools and resources	✓
	PE2.3 Application of systematic engineering synthesis and design processes	✓
	PE2.4 Application of systematic approaches to the conduct and management of engineering projects	
PE3: Professional and Personal Attributes	PE3.1 Ethical conduct and professional accountability	
	PE3.2 Effective oral and written communication (professional and lay domains)	✓
	PE3.3 Creative, innovative and pro-active demeanour	✓
	PE3.4 Professional use and management of information	✓
	PE3.5 Orderly management of self, and professional conduct	✓
	PE3.6 Effective team membership and team leadership	